System-Level Requirements of DC-DC Converters for Dynamic Power Supplies of Power Amplifiers

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***Abstract*- The energy efficiency of battery-operated portable applications can be improved by increasing the efficiency of power amplifiers (PAs). By dynamically changing the supply voltage from the fixed battery supply using a DC-DC converter, the PA can be operated with high efficiency during power back-off. This paper presents the system level requirements for a buck converter and other blocks in a dynamic power supply scheme for PA. Simulation results for the effects of ripple in the power supply of the PA and delay mismatch using behavioral models of constituent blocks and circuit-level PA have been presented.**

I. INTRODUCTION

Efficient radio-frequency (RF) power amplifiers (PAs) are highly desirable in battery-operated systems such as cellular phones, because PAs typically dominate the power consumption of such devices. The amplification of non-constant envelope RF modulation such as OQPSK requires linear PAs, which are inherently less power efficient. To maintain linearity and minimize distortion, the power amplifiers need to be operated in class-A configuration, which exhibit a maximum theoretical efficiency of only 50% when the output signal swings from rail to rail. Therefore, to operate the PA at its high efficiency range, the power supply must change dynamically, depending on the amplitude of the output signal.

To regulate the battery into a dynamically variable voltage, high performance power efficient voltage regulators are required. Because of their high-efficiency, switching converters are preferred over linear regulators, in spite of complexity, cost and noise [1]. Assuming that the battery voltage is sufficiently high for the PA during maximum power transmission, even when the battery is almost fully discharged, a step-down (buck) converter would be needed for lower voltages, during power back-off operation mode. Therefore, all the discussion throughout this paper is in reference to a DC-DC buck converter.

The control signal for the DC-DC converter can be derived either from the RF input signal or can be taken out from the base band section of the radio transmitter. From an integrated power amplifier perspective, the former signal seems to be most promising because it can be independently designed, without any knowledge of the transmitter architecture. On the other hand, overall transmitter architecture knowledge is required to access and process the base band signal. Therefore, the dynamic supply selection scheme considered in this work involves the task of obtaining the envelope of the RF input using a directional coupler and envelope detector, generating the controlling signal for the DC-DC converter and changing the supply voltage for the PA.

In this research, we have investigated the requirements of individual building blocks, i.e., the DC-DC converter and dynamic supply selection mechanism. A circuit level net-list for the PA is used for simulation, where as other blocks are replaced by behavioral models.

The organization of the paper is as follows. An overview of the previous work and objective of the research is presented in Section II. In Section III, the simulation set-up for the overall scheme, combination of behavioral models and circuit level net-lists, are presented. Simulation results for the controlling scheme and summary are presented in Sections IV and V, respectively.

II. OVERVIEW OF THE OVERALL SCHEME

A. Previous Work

Several techniques have been reported in the literature with regard to improving the efficiency and linearity of the PA. Raab, et. al. [2] have proposed an L-band transmitter based upon Kahn envelope-elimination and restoration (EER) technique, which combines a nonlinear RF PA with an envelope amplifier to implement a high efficiency linear RF PA. The schematic of such a scheme is shown in Figure 1.

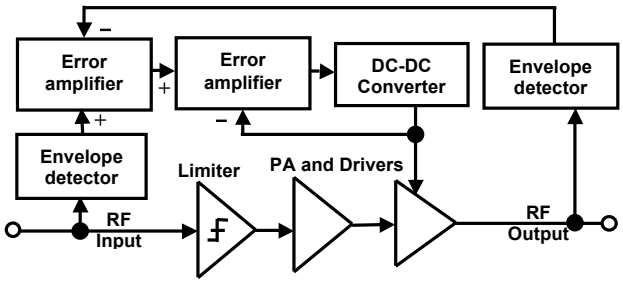

Figure 1. Schematic of Kahn EER technique.

A limiter in the forward path generates a constant amplitude signal, retaining only the phase information that is amplified by the first stage of the amplifier. An envelope detector detects the amplitude of the signal and controls the DC-DC converter output. To restore the amplitude information, the DC-DC converter, according to the envelope of the input signal, varies the supply to the RF stage dynamically. Su and McFarland have reported an integrated circuit implementation of the above scheme in [3]. A delta modulated power supply was used for the DC-DC converter instead of using any PWM controlling scheme.

Another technique for improving the efficiency of the RF power amplifiers without the use of complex envelope restoration, proposed by Saleh and Cox [4], is to dynamically vary the gate bias, in step with the envelope of the incoming signal, keeping supply voltage constant. The quiescent current of the amplifier is optimally adjusted –lowering the input

current when the input signal is small. The schematic of this scheme is shown in Figure 2.

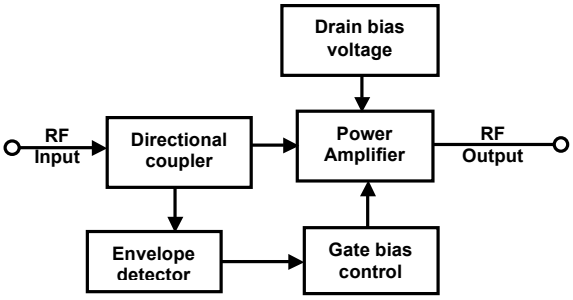

Figure 2. Schematic of the scheme proposed by Saleh and Cox [4].

A dc-dc boost converter is used to provide the supply voltage of a MESFET power amplifier is reported in [5]. The authors report that by using the boost converter operating at 10 MHz, the power amplifiers operate with higher efficiency with high V_{DD} due to finite saturation voltage of the power amplifier, and as the input voltage drops, due to battery discharge, the required high-voltage level can still be maintained, even as the battery is running towards exhaustion.

This scheme assumes that the maximum output signal amplitude of the RF PA is higher than the battery supply voltage. However, during power back-off mode and voice only mode the power amplifier can be operated at a voltage less than the battery voltage. Essentially, the battery voltage needs to be stepped-down, rather than stepped-up to operate the PA in all required modes of operation. Under these circumstances, by using the scheme proposed in [5], the PA is supplied with full battery voltage, even if not required. Therefore, input dc power remaining constant, the efficiency of PA degrades with reduced output signal power.

In the work reported in [6], the authors have demonstrated that digital control of the DC-DC converter, coupled with digital pre-distortion of the amplifier input signal can improve the amplifier linearity while optimizing power efficiency. Application of DSP allows flexibility for power supply selection, ability to equalize the delay and the frequency response of the DC-DC converter. The DSP can implement a variety of algorithms for system optimization. However, this approach requires integrated design of the overall transmitter, since functions of the DSP and PA are closely coupled.

A radio-frequency PA targeted for code division multiple access (CDMA) using dynamic envelope tracking (ET) technique is reported in [7]. The envelope detector detects the profile of the modulated signal and generates a control signal for the DC-DC converter based on the rms value of the modulated signal. In power back-off mode, the voltage is reduced below the battery voltage. The efficiency of the amplifier is increased since the amplifier is operated close to gain compression, where it is inherently most efficient. The power consumed by the amplifier during back-off is less than would be the case if it were operated at higher voltage.

A summary of the schemes described earlier is presented in Table 1.

Table 1. Summary of PA efficiency improvement schemes with dynamic power supply schemes.

Scheme	Advantages	Disadvantages
Kahn EER [2]	Efficiency of the scheme can be very high.	Difficult to retain envelope information accurately at high frequencies.
Gate biasing [4]	Efficiency can be improved, but as high by changing supply voltage.	Control overhead high but not much power saving.
Boost converter [5]	PA can be supplied with higher voltage even during battery is close to fully discharged.	No power saving if battery voltage is sufficient for the PA.
DSP control [6]	Flexible algorithm can be employed. High-speed converter is not required.	Overall transmitter architecture is required-not suitable for stand-alone PA.

B. Objective of this research

From an integrated power amplifier perspective, the scheme proposed in [7] seems to be the most promising one. For faithful amplification of the input signal, the output voltage should be sufficiently large to keep it from being distorted. However, in practice, the DC-DC converter takes a finite amount of time to respond to the control signal. This leads to a requirement of delay in the RF input signal to the PA, equal to the time needed for the DC-DC converter to adjust the supply voltage to the PA. The output ripple voltage of the converter be kept small to prevent it from interfering with the operation of the PA and contributing noise to the overall system. The functional representation of the scheme that is considered in this work is shown in Figure 3.

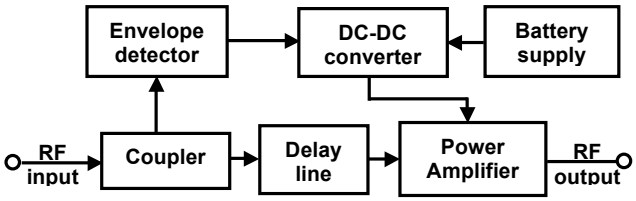

Figure 3. Functional block diagram of the overall scheme.

The performance of the PA is evaluated with respect to the following factors: (a) ripple in the power supply for the PA, due to the converter, and (b) delay mismatch between the DC-DC converter and the delay line.

III. MODELING AND IMPLEMENTATION

To evaluate the effects of delay and output ripple on the performance of the PA, the system was simulated using HP-ADS simulator. The PA works as a load for the DC-DC converter. For designing the converter, accurate modeling of power amplifier is needed. The power amplifier considered in this work is a two-stage BJT amplifier operating in class-A configuration. The biasing and supply of the second stage was only varied –to maximize efficiency and minimize distortion, while biasing and supply of the first stage was kept constant.

A simplified schematic of the PA and its equivalent circuit as a load for the converter are shown in Figure 4.

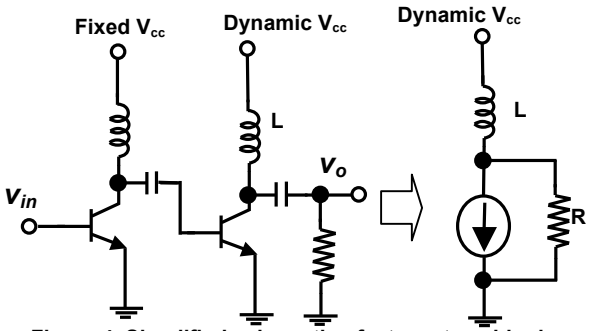

Figure 4. Simplified schematic of a two-stage bipolar power amplifier and its equivalent circuit as load for the DC-DC converter.

The value of inductance L in the equivalent circuit is the same as that of the RF choke. This is small compared to the filter inductance in the DC-DC converter, which sets its response time. Resistance R is given by:

$$R = R_C + \frac{V_{CEQ}}{I_{CQ}}, \quad (1)$$

where R_C is the collector resistance, V_{CEQ} is the collector emitter bias voltage, and I_{CQ} is the collector bias current.

Different controlling mechanisms [8] can be used for feedback control of the DC-DC converter. Because of simplicity of the control loop and fixed operating frequency, a voltage-mode DC-DC converter is used where the PWM controller and the error amplifier are realized using macro-models, the schematic of which is shown in Figure 5.

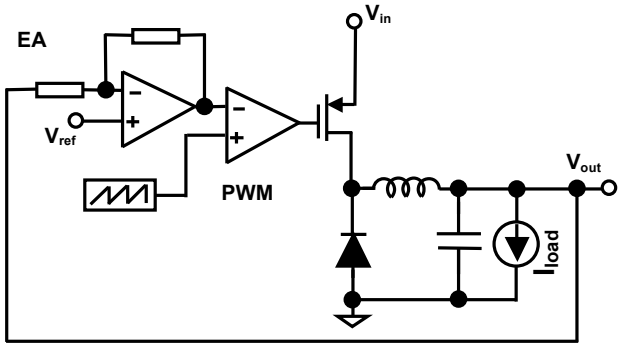

Figure 5. Buck converter with voltage- mode control.

The limit on the bandwidth of the envelope signal that can be successfully followed by the converter depends on the closed-loop bandwidth of the DC-DC converter. According to the sampling theorem, to reproduce the signal frequency, the sampling frequency needs to be at least twice that of the signal frequency. Since the bas-band signal bandwidth in CDMA-IS 95 standard is 1.23 MHz, the closed loop bandwidth of the DC-DC converter should be at least 2.46MHz ($2*f_{BW}$). This limit requires that the switching frequency of the DC-DC converter should be much higher than the base band signal frequency. A switching frequency of 10 MHz is chosen in this case.

The envelope detector used is an amplitude demodulator, the schematic of which is shown in Figure 6. The values of R and C for the envelope detection circuit are determined from the carrier frequency ($f_{carrier}$) and base band signal frequency (f_{signal}). The relation is given by:

$$f_{signal} < \frac{1}{2\pi R C} << f_{carrier}. \quad (2)$$

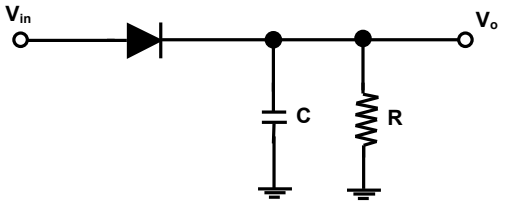

Figure 6. Schematic of the envelope detector.

IV. SIMULATION RESULTS

The performance of the PA in the overall scheme is affected by two factors: the ripple in the power supply to the PA and differential delay between the delay line and DC-DC converter. These non-idealities in the dynamic power supply result in generation of unnecessary spurious signals. The PAs in modern digital modulation schemes having multiple carrier frequency such as CDMA are characterized by the specification called adjacent power channel power ratio (ACPR), or spectral regrowth. ACPR is defined as the measured power in an adjacent communications channel of specified bandwidth relative to the power in the main channel of specified bandwidth (Figure 7). It is basically a measure of power in the side-lobes due to all the inter-modulation distortion (IMD) products relative to the desired channel. Therefore, in this work, the PA is characterized by its ACPR characteristics.

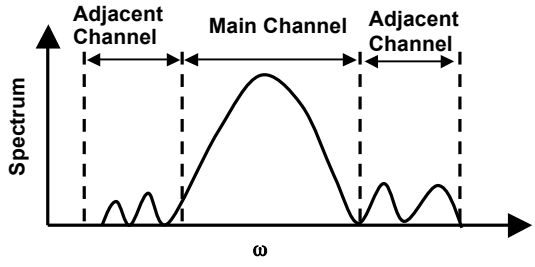

Figure 7. Illustration of ACPR.

1. Effect of ripple in the power supply of the PA

The effect of ripple in the supply of the PA was simulated by using an ac source of 10 MHz along with a DC source for the supply voltage of the PA. In addition to 1st ACPR at 885 KHz and 2nd ACPR at 1980 KHz, the third ACPR at 10MHz is also considered as a performance parameter, because the ripple frequency of 10 MHz in the power supply can create a noise spectrum in the region +/– 10 MHz offset from the carrier frequency. A summary of the simulation results with variation in ripple voltage is presented in Table 2.

With the increase in ripple voltage, the output power decreases for the same input power –the power gain decreases. While the 1st ACPR performance degrades with increase in ripple voltage, the 2nd ACPR performance improves. Another performance of interest, ACPR at 10 MHz

offset actually degrades, but remains within the requirement of IS-95 standard.

Table 2. Effect of supply voltage ripple on the performance of the PA (P_{in} = 0 dBm, V_{supply}= 2.5 V).

Ripple	Output power (dBm)	1st ACPR (dBc)	2nd ACPR (dBc)	ACPR @ 10MHz (dBc)
0 mV	28.78	-37.81	-58.11	-79.66
25 mV	28.64	-37.26	-59.03	-75.42
125mV	28.57	-37.12	-59.35	-74.67
250mV	28.32	-36.48	-61.26	-71.64

2.Effect of mismatch of delay of the DC-DC converter and delay line

The DC-DC converter employs a low-pass output filter to suppress the switching frequency and its harmonics. Delay is inherent in any filter and increases as bandwidth decreases. To avoid loss of modulation accuracy and minimize distortion, the supply voltage applied to the PA must be in-phase with the envelope, or lead it, and of sufficient magnitude to prevent clipping. Therefore, a delay line needs be inserted in the path of the RF signal to the power amplifier assuming that the converter is not faster than the PA. In practical circuits, it is very much possible that there will be delay mismatch between the two paths leading to performance degradation of the PA. Simulation results are presented in Table 3.

Table 3. Effect of delay mismatch on the performance of the PA with dynamic power supply.

Input power (dBm)	Delay mismatch	Output power (dBm)	1st ACPR (dBc)	2nd ACPR (dBc)
0	0	21.87	-32.31	-41.91
	10ns	21.61	-31.94	-39.64
	100ns	19.44	-28.25	-34.95
-10	0	16.55	-46.43	-54.59
	10ns	16.23	-42.54	-50.23
	100ns	16.31	-38.78	-48.92

From the simulation results, it is seen that with 0 dBm input power, the PA operates close to gain saturation, introducing more non-linearity –the ACPR requirement for CDMA IS-95 are not satisfied even with no delay mismatch. However, with reduced input power of –10dBm, the PA exhibits linear operation and the ACPR requirements are met with the dynamic supply voltage. For 10ns differential delay, the performance of PA degrades, but not as drastically as with delay mismatch of 100ns. Essentially, this leads to the fact that with power back-off the PA exhibits enough linearity to meet ACPR requirements with dynamic power supply.

With increase in delay mismatch, the linearity degrades resulting in reduction in output power. The spectrum spreads resulting in more power distribution in the side-lobes – ACPR performance degrades. Therefore, the delays need to be matched to an extent such that the ACPR performance requirement is satisfied.

V. SUMMARY

The effects of non-idealities in the building blocks for a dynamic power supply power amplifier have been identified and their effects on the power amplifier performance are investigated. Simulation results showing the effects of delay mismatch, effect of ripple on the supply line, have been presented. The switching frequency of the DC-DC converter must be high such that the power supply to the PA can be changed according to the envelope of the RF signal. The effect of ripple in the power supply to the PA is not as severe as the effect of delay mismatch. The delay mismatch between the converter and the delay line must be kept less than 10ns to meet the ACPR requirements. Our future effort will be to design an integrated solution of the complete system.

VI. ACKNOWLEGDEMENTS

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