A Comprehensive Power Analysis and a Highly Efficient, Mode-Hopping DC-DC Converter

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***Abstract*- A comprehensive power analysis, keeping integrated circuits in mind, is presented while highlighting all conduction, switching, and dynamic power losses in a DC-DC converter. Synchronous rectification, zero-voltage switching, mode-hopping, and variable frequency operation are evaluated. The efficiency for constant frequency CCM, constant frequency DCM, and constant on-time, variable frequency DCM techniques is analyzed and the optimum technique is derived. It is concluded that a mode-hopping converter employing an asynchronous, constant on-time, variable frequency DCM operation for low output currents and a synchronous, constant frequency CCM operation for high load currents yields the best efficiency performance.**

1. INTRODUCTION

The demand for high efficiency DC-DC converters is increasing dramatically, especially for use in battery-operated devices such as cellular phones and laptop computers. In these devices, it is intrinsic to extend battery life. By employing DC-DC converter power-saving techniques, power efficiency can be significantly increased, thereby extending battery life.

Numerous techniques have been proposed over the years to increase the power efficiency of DC-DC converters. Some of the more significant techniques are analyzed and discussed in Section 3. Section 4 discusses maximum efficiency using different modulation techniques. The optimum modulation technique is derived and simulation results are presented. But first, a comprehensive power analysis is presented in Section 2 to help understand where the power losses in the converter originate.

2. POWER ANALYSIS

Power is dissipated in the converter by the following: load current, RMS current, controller current, switching current, and thermal losses. Through minimization of the losses in these areas, the overall efficiency of the converter will increase. Figure 1 shows a buck converter with the associated parasitic components.

2.1 Load Current

The load current induces power losses in the load, the inductor, and the switches. The following equations govern the load current losses:

$$P_{Load} = I_{Load} \cdot V_{Out}, \quad (1)$$

$$P_{L\_ESR} = I_{Load}^2 \cdot R_{L\_ESR}, \quad (2)$$

$$P_{HS} = d \cdot I_{Load}^2 \cdot R_{SW}, \quad (3)$$

and

$$P_{LS} = (1-d) \cdot I_{Load}^2 \cdot R_{SW}, \quad (4)$$

where d is the duty cycle and R_{SW} is the transistor ON resistance. Or, if only a diode is used for the low side (asynchronous), then

$$P_{LS} = (1-d) \cdot I_{Load} \cdot V_D. \quad (5)$$

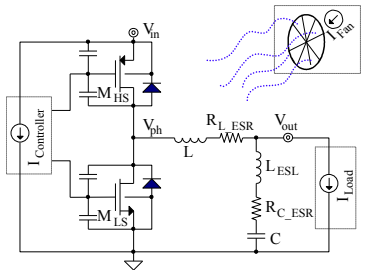

Figure 1. Buck Converter & Associated Parasitic Components.

The MOSFET body diode losses during the dead time must also be taken into account,

$$P_{LS} = 2 \cdot \left(\frac{t_{dead}}{\tau} \right) \cdot I_{Load} \cdot V_{DLS}. \quad (6)$$

Dead time is required to prevent both switches from being ON simultaneously. If this occurs, a short circuit path is established and significant shoot-through current from the supplies results.

2.2 RMS Current

The RMS current dissipates power through the capacitor, the inductor, and the switches,

$$P_{ESR} = I_{RMS}^2 \cdot (R_{L\_ESR} + R_{C\_ESR}), \quad (7)$$

$$P_{HS} = d \cdot I_{RMS}^2 \cdot R_{SW}, \quad (8)$$

and

$$P_{LS} = (1-d) \cdot I_{RMS}^2 \cdot R_{SW}. \quad (9)$$

Or, in the asynchronous case,

$$P_{LS} = (1-d) \cdot I_{RMS} \cdot V_D, \quad (10)$$

and

$$P_{DLS} = 2 \cdot \left(\frac{t_{dead}}{\tau} \right) \cdot I_{RMS} \cdot V_{DLS} \quad (11)$$

for the MOSFET body diode.

2.3 Controller Current

The current through the controller ultimately leads to gate-drive and quiescent-current power losses. When the gate of the transistor is charged/discharged, power is dissipated. Since the gate-drive loss is independent of the load current, this loss will mainly become evident in light-loading conditions [6]. The quiescent power loss can be expressed by

$$P_{Q\_Cont} = I_{Controller} \cdot V_{In}. \quad (12)$$

If a few reasonable assumptions are made ($10 \cdot C_{gd} \approx C_{gs}$, $A_{linear} \approx 10$, and $t_{Miller} \approx t_{on}/3$), the switching loss through the parasitic capacitors can be expressed by

$$P_{C\_Cont} = 16 \cdot C_{gs} \cdot V_{In}^2 \cdot \left(\frac{f}{3}\right). \quad (13)$$

2.4 Switching Current

During switching transitions, voltage and current cross over, resulting in power loss. By making the reasonable assumption that $I_{LS} \approx I_{L,+Peak}(1\text{-}t/t_x)$ and $V_{LS} \approx V_{in}(1\text{-}t/t_x)$ where t_x is the total rise and fall time, the power lost in the switches is approximately

$$P_{Switch} \approx I_{Load} \cdot V_{in} \cdot \left(\frac{t_x}{\tau}\right). \quad (14)$$

2.5 Thermal Losses

Thermal losses in a converter are important, but often overlooked. If the converter overheats, a fan and a current to drive the fan will be required, which leads to more power consumption. If only a heat sink is required, this still raises the cost, size, and weight of the converter. Also, as the temperature increases, the ON resistance of the MOSFET switches also increases, leading to greater power dissipation in the switches.

2.6 Summary

At high load currents, the main contributor to power loss is the load current (conduction losses through the switches, diodes, and ESR). At low loading conditions, the main power losses are a function of frequency, which are nearly load independent (switching losses). At low load currents, synchronous converters incur more conduction losses than the asynchronous counterpart.

3. POWER SAVING TECHNIQUES

3.1 Synchronous Rectification

The classical means of improving power efficiency in DC-DC converters is to replace the Schottky (Figure 2a) with a MOSFET synchronous rectifier (Figure 2b) [1]. By replacing the rectifying diode with a MOSFET, the forward voltage drop decreases, thereby reducing power losses.

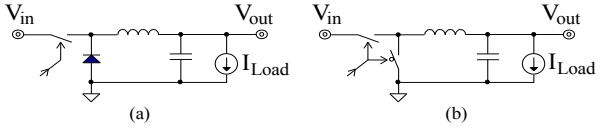

Figure 2. (a) Asynchronous and (b) Synchronous Buck Converters.

However, while this technique may decrease conduction losses, it will add additional switching losses. In applications where a high switching frequency or high output current is desired, this technique proves to be less efficient than the traditional topology. Figure 3 [2] shows that at high frequencies the asynchronous topology becomes more efficient than the synchronous topology [2].

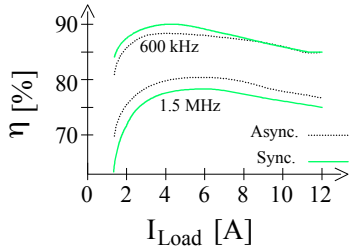

Figure 3 [2]. Converter efficiency in async. and sync. modes at different operating frequencies.

This phenomenon results because the delay of the converter becomes a significant portion of the period, thereby losing power through the body diodes.

Overall, [2] found that for low voltage applications requiring small size and fast response, the regular asynchronous buck topology is preferred, in regards to efficiency and overall cost.

3.2 Zero Voltage Switching

In a hard-switched converter, power will be lost due to the charging of the parasitic capacitances of the switch and shoot-through current (if little to no dead time is used) or reverse recovery loss (if dead time is used). In a zero-voltage switched converter (Figure 4 [6]), the parasitic capacitances are charged and discharged through the use of the output inductor acting as a current source [6]. A shunt capacitor is added at node V_1 to slow the transitions. If appropriate dead times are set, the transistors are switched when $V_{ds} = 0$, thus eliminating switching losses.

If switch LS is switched off after the inductor current reverses, and switch HS remains off, the inductor will act like a current source and charge node V_1 [6]. The HS switch is then turned on when $V_1 = V_{in}$, and the transition occurs when V_{ds} of the HS switch is zero, resulting in a lossless transition. A more extensive analysis of ZVS can be found in [6], and [3] provides analysis of both quasi- and multi-resonant approaches.

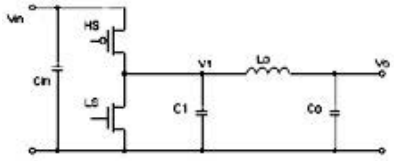

Figure 4 [6]. ZVS Buck Circuit.

Due to low switching losses, ZVS circuits can be operated at very high frequencies, thus substantially reducing the size and weight of the converter [3]. However, it is difficult to ensure proper dead times for ZVS operation across all loading conditions.

3.3 Mode-Hopping

Synchronous Continuous Conduction Mode (CCM) operation during heavy loads and asynchronous Discontinuous Conduction Mode (DCM) operation during light loads leads to optimized efficiency, as shown in Figure 5 [4]. Consequently, mode-hopping between CCM and DCM modes is recommended, depending on the load current.

To mode-hop, [4] makes use of a digital PWM controller to control the operational mode of the converter, based on the characteristics of the output current. For example, when loading conditions are light, the converter operates in asynchronous DCM mode. But when loading is high, the converter operates in synchronous CCM. Detecting this conversion point, however, leads to higher complexity and possible spurious signals.

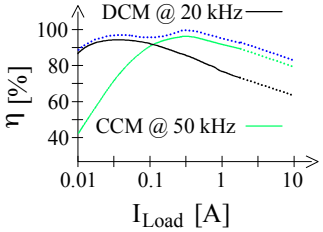

Figure 5 [4]. Converter Efficiency in CCM and DCM.

3.4 Variable Frequency

A fourth method is to vary the frequency as a function of a load current (decreasing the switching frequency when loading conditions are light). The graphs in Figure 6 show the losses in a fixed frequency converter and a variable frequency converter [5]. As shown, by decreasing the frequency when loading conditions are light, a significant reduction in power loss is realized ([5] offers a detailed analysis).

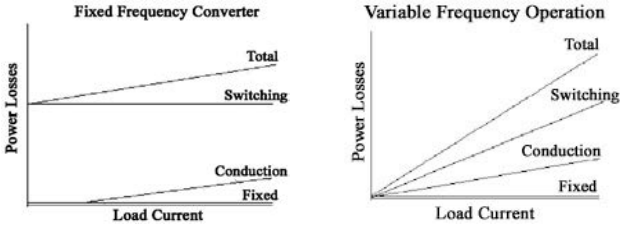

Figure 6 [5]. Fixed & Variable Frequency Converter Losses.

3.5 Summary

It was shown that for high frequencies, asynchronous mode yields higher efficiency than synchronous mode. ZVS yields high efficiency and can be operated at high frequencies, but to ensure ZVS operation over a wide range of loading conditions is complex. Mode-hopping was shown to be a good technique to achieve a high efficiency over a wide range of loads, but also has high complexity. Variable frequency operation, which is directed toward lowering the frequency during times of low loading, was shown to increase overall efficiency, especially during very low loading conditions which is prevalent in cell phones, DSP, and portable applications.

4. MAXIMUM EFFICIENCY

The power efficiency in a given buck converter for CCM PWM constant frequency, DCM PWM constant frequency, and DCM constant on-time variable frequency modulation techniques are optimized and the results are compared. The following simplifying model, based on the predominant losses, is used for deriving the overall power losses in DC-DC converters:

$$P_{Loss} = P_{Cond} + P_{SwitchLoss} = R_{eq} \cdot i^2_{RMS} + A \cdot f \qquad (15)$$

where R_{eq} is the equivalent resistance of the system, i_{rms} is the RMS value of the inductor current, A is the switching power loss factor and f is the operating frequency. The conduction loss of R_{ESR} is assumed to be negligible, which is reasonable if high quality capacitors with low R_{ESR} are used [6]. It is also assumed that the switching loss is independent of the output current, which is true if the turn off overlapping loss and inductor core losses are negligible [7].

In both CCM and DCM modes, when the high-side MOSFET is ON, the total resistance causing conduction losses is roughly $R_1 = R_s + R_{on1} + R_L$, and the total resistor value when the low-side MOSFET is ON is $R_2 = R_{on2} + R_L$, where R_{on1} and R_{on2} are MOSFET ON resistances, R_L is the inductor resistance, and R_s is the source resistance.

Consequently, in CCM operation, the conduction loss can be computed as $P_{cond} = R_1\, i^2_{rms1} + R_2\, i^2_{rms2}$ where i_{rms1} is the RMS value of I_L when the high-side MOSFET is ON and i_{rms2} is the RMS value of I_L when the low-side MOSFET is ON. Thus,

$$P_{condCCM} = R_{eqCCM} \cdot i^2_{RMS\_CCM} \qquad (16)$$

where $R_{eqCCM} = (R_1 (V_o/V_{in}) + R_2 (1 - V_o/V_{in}))$, $i^2_{rmsCCM} = I^2_o + \Delta I^2_L / 12$, I_o is the load current, and ΔI_L is the value of the ripple inductor current.

Similarly, during the DCM operation, the conduction losses can be computed as

$$P_{condDCM} = R_{eqDCM} \cdot i^2_{RMS\_DCM} \qquad (17)$$

where $R_{eqDCM} = (R_1 (V_o/V_{in}) + R_2 (1 - V_o/V_{in}))$ and $i^2_{rmsDCM} = I^2_p/3(1 - t_d/T)$. Since the equivalent resistor value turns out to be the same for both CCM and DCM, R_{eq} is used from now on to represent the equivalent resistance of either mode. The efficiency of the DC-DC converter can be stated as

$$Efficiency = \eta = \frac{P_{out}}{P_{out} + P_{loss}}$$

$$= \frac{V_o I_o}{V_o I_o + R_{eq} i^2_{rms} + Af} = \frac{1}{1 + \frac{R_{eq} i^2_{rms} + Af}{V_o I_o}} = \frac{1}{1+\gamma}, \qquad (18)$$

where $$\gamma = \frac{R_{eq} i^2_{rms} + Af}{V_o I_o}. \qquad (19)$$

Optimizing efficiency means minimizing efficiency parameter γ.

4.1 CCM Constant Frequency PWM

In CCM constant frequency PWM, $i^2_{rmsCCM} = I^2_o + \Delta I^2_L / 12$. Substituting i_{rmsCCM} in (19) gives

$$\gamma_{CCM} = R_{eq} \frac{I_o^2 + \Delta I_L^2 / 12}{V_o I_o} + \frac{Af}{VoIo}$$

$$= R_{eq} I_o / V_o + R_{eq} \frac{k^2}{12 f^2 V_o I_o} + \frac{Af}{V_o I_o}, \qquad (20)$$

where $\Delta I_L = \left(\frac{V_{in} - V_o}{L}\right)\frac{V_o}{V_{in}} T = k/f$ and $k = \left(\frac{V_{in} - V_o}{L}\right)\frac{V_o}{V_{in}}$.

By setting $d\gamma_{CCM}/dI_o = 0$, the minimum value of γ is obtained as

$$\gamma_{CCM} = 2\frac{R_{eq}}{V_o}\left(\frac{Af}{R_{eq}} + \frac{k^2}{12 f^2}\right)^{0.5}, \qquad (21)$$

when $I_o^2 = Af/R_{eq} + k^2/12f^2$. Minimizing by setting $d\gamma_{CCM}/df = 0$ results in

$$\gamma_{CCM} = \frac{(6 \cdot A)^{1/3} \cdot R_{eq}^{2/3} \cdot k^{1/3}}{V_o} \qquad (22)$$

when $f = \frac{k^{2/3} \cdot R_{eq}^{1/3}}{(6 \cdot A)^{1/3}}$.

4.2 DCM Constant Frequency PWM

In DCM, the RMS value of inductor current is

$$i^2_{rmsDCM} = \left(\frac{2}{3}\right) \cdot I_O \cdot I_P = 2 \cdot \sqrt{2/3} \cdot I_O^{3/2} \cdot \Delta I_L^{1/2}$$

$$= 2 \cdot \sqrt{2/3} \cdot I_O^{3/2} \cdot \left(\frac{k}{f}\right)^{1/2} \qquad (23)$$

Substituting in (19) gives

$$\gamma = R_{eq} \cdot \frac{\left(2 \cdot \sqrt{2/3} \cdot I_O^{1/2} \cdot (k/f)^{1/2}\right)}{V_O} + \frac{A \cdot f}{V_O \cdot I_O}. \qquad (24)$$

By setting $d\gamma/dI_o = 0$, the minimum value of γ is obtained as

$$\gamma_{DCM} = \frac{(6 \cdot A)^{1/3} \cdot R_{eq}^{2/3} \cdot k^{1/3}}{V_O}, \qquad (25)$$

when $I_O = A^{2/3} \cdot \left(\frac{3}{\sqrt{2}}\right)^{2/3} \cdot R_{eq}^{-2/3} \cdot k^{-1/3} \cdot f$.

4.3 Constant on time, variable frequency DCM

In this method [5], the high-side switch is on until the inductor current reaches a fixed value of I_p. The modulation frequency is variable and is directly proportional to the output current. As the output current decreases the operating frequency also decreases and this results in lower switching losses. So, intuitively, this method should result in higher efficiency. The operating frequency is evaluated as [5]

$$f = \frac{2I_o}{I_p^2}\left(\frac{V_{in} - V_o}{L}\right)\frac{V_o}{V_{in}} = \frac{2I_o}{I_p^2}k. \qquad (26)$$

Substituting i_{rmsDCM} from (9) and frequency from (12) into (5) results in

$$\gamma = R_{eq}\frac{2}{3}\frac{I_p}{V_o} + \frac{2Ak}{I_p^2 V_o}. \qquad (27)$$

The efficiency parameter γ is independent of the output current, but is a function of I_p, the peak inductor current[5]. By setting $d\gamma/dI_p=0$, the minimum value of γ is obtained as

$$\gamma = (6A)^{1/3} R_{eq}^{2/3} k^{1/3} / V_o \qquad (28)$$

when $I_p = (6A)^{1/3} R_{eq}^{-1/3} k^{1/3}$.

Consequently, for a given DC-DC converter with known values of A, R_{eq}, L, V_{in} and V_o, the maximum attainable efficiency for all three methods is the same ($\gamma_{CCM} = (6A)^{1/3} R_{eq}^{2/3} k^{1/3} / V_o$) as derived in equations (22), (25) and (28).

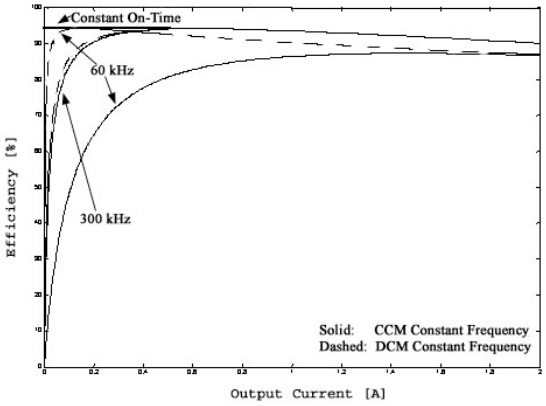

Figure 7. Efficiency of Modulation Techniques.

However, in CCM constant frequency mode the maximum efficiency occurs only for a particular combination of current and frequency. In DCM constant frequency mode, there is a particular output current for any given frequency at which the efficiency is maximum. With the constant on-time method, maximum efficiency is obtained for any output current, provided that the proper value of I_p is chosen; however, the maximum output current is limited to $I_o = I_p/2$.

The above analysis suggests mode hoping and using a constant on-time, variable frequency for low output current to $I_o = I_p/2$. For $I_o > I_p/2$ constant frequency PWM is used as it is reported but not proven in [8]. Figure 7 shows a simulation of efficiency versus output current in a buck DC-DC converter with A=0.1 watt/1Mhz, R_{eq}=0.1 Ω, V_{in} =5v, V_o=2v and k=3e5 (L=4uH).

5. CONCLUSIONS

A comprehensive power analysis of a DC-DC converter was presented, analyzing switching, conduction, and dynamic power losses. Asynchronous mode was shown to yield higher efficiency than synchronous mode at high frequencies. ZVS was shown to have high efficiency, but complex operation. Both mode-hopping and variable frequency operation were shown to be important techniques in improving the efficiency of the converter. Finally, the optimum modulation technique was derived and proven.

Therefore, it is concluded that a mode-hopping DC-DC converter employing asynchronous, constant on-time, variable frequency DCM operation for low output currents (up to $I_o = I_p/2$) and synchronous, constant frequency CCM operation for high load currents (for $I_o > I_p/2$) yields the best efficiency performance.

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