

# *Switched-Inductor Power Supplies*

*By*

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## *Contents*

	<b>Page</b>
<b>List of Figures</b>	vii
<b>List of Abbreviations</b>	ix
<b>1. Transfer Media</b>	1
1.1. Inductor	1
A. Ideal Inductor	1
B. Actual Inductor	2
C. Optimal Inductor	3
1.2. Transformer	3
A. Ideal Transformer	3
B. Actual Transformer	5
<b>2. Switched Inductors</b>	6
2.1. Static Power-Supply Applications	6
2.2. Inductor Current	6
2.3. Duty Cycle	7
A. Ohmic Losses	8
2.4. Continuous Conduction	9
2.5. Discontinuous Conduction	10
2.6. CMOS Implementations	11
2.7. Design Limits	13
<b>3. Buck–Boost</b>	14
3.1. Ideal Buck–Boost	14
A. Power Stage	14
B. Duty-Cycle Translation	15
C. Power	16
3.2. Asynchronous Buck–Boost	17
A. Power Stage	17
B. Duty-Cycle Translation	18
C. Conduction Modes	20
3.3. Synchronous Buck–Boost	21
A. Power Stage	21
B. Duty-Cycle Translation	23
C. Conduction Modes	25
D. Diode Conduction	26
<b>4. Buck</b>	27
4.1. Ideal Buck	27
A. Power Stage	27
B. Duty-Cycle Translation	28
C. Power	29

4.2. Asynchronous Buck	29
A. Power Stage	29
B. Duty-Cycle Translation	29
C. Conduction Modes	30
4.3. Synchronous Buck	32
A. Power Stage	32
B. Duty-Cycle Translation	32
C. Conduction Modes	33
D. Diode Conduction	34
<b>5. Boost</b>	<b>34</b>
5.1. Ideal Boost	34
A. Power Stage	34
B. Duty-Cycle Translation	35
C. Power	36
5.2. Asynchronous Boost	36
A. Power Stage	36
B. Duty-Cycle Translation	36
C. Conduction Modes	37
5.3. Synchronous Boost	39
A. Power Stage	39
B. Duty-Cycle Translation	39
C. Conduction Modes	40
D. Diode Conduction	41
<b>6. Flyback</b>	<b>41</b>
6.1. Ideal Flyback	41
A. Power Stage	41
B. Duty-Cycle Translation	43
C. Power	44
D. Variants	44
E. Snubbers	44
6.2. Asynchronous Flyback	47
A. Power Stage	47
B. Duty-Cycle Translation	48
C. Conduction Modes	49
6.3. Synchronous Flyback	50
A. Power Stage	50
B. Duty-Cycle Translation	51
C. Conduction Modes	53
D. Diode Conduction	53
<b>7. Summary</b>	<b>53</b>

## *List of Figures*

	<b>Page</b>
Figure 1. Magnetizing inductor.	2
Figure 2. Ideal transformer.	4
Figure 3. Actual transformer.	5
Figure 4. Phases of the switched inductor.	6
Figure 5. Inductor voltage and current in dc-supplied chargers and regulators.	7
Figure 6. Inductor current with Ohmic losses.	8
Figure 7. Inductor current in continuous conduction.	9
Figure 8. Inductor current in discontinuous conduction.	10
Figure 9. Ideal buck–boost.	15
Figure 10. Asynchronous buck–boost.	17
Figure 11. Asynchronous buck–boost voltages.	19
Figure 12. Discontinuous-conduction waveforms.	20
Figure 13. Drained and disconnected asynchronous buck–boost inductor.	21
Figure 14. Synchronous buck–boost.	22
Figure 15. Continuous conduction with non-reversing inductor current.	23
Figure 16. Continuous-conduction with reversing inductor current.	26
Figure 17. Schottky-clamped synchronous buck–boost.	27
Figure 18. Ideal buck.	28
Figure 19. Asynchronous buck.	29
Figure 20. Drained and disconnected asynchronous buck inductor.	31
Figure 21. Synchronous buck.	32
Figure 22. Ideal boost.	35
Figure 23. Asynchronous boost.	36
Figure 24. Drained and disconnected asynchronous boost inductor.	38
Figure 25. Synchronous boost.	39
Figure 26. Ideal (supply-switched) flyback.	42
Figure 27. Continuous-conduction waveforms in the flyback.	42
Figure 28. Ground- and supply-switched flyback variations.	45
Figure 29. Input-damped flyback.	45
Figure 30. Input-clamped flyback.	46
Figure 31. Asynchronous flyback.	47
Figure 32. Discontinuous-conduction waveforms in the flyback.	49
Figure 33. Synchronous flyback.	50

### B. Actual Transformer

In practice, coupled inductors access a fraction of the magnetic field they share. So when decomposed into the pieces that actually couple:  $L_1$  and  $L_O$ , and the ones that do not:  $L_1'$  and  $L_O'$ , like Fig. 3 illustrates, only a  $k_{CI}$  fraction of the input couples to a  $k_{CO}$  fraction of the output:

$$k_{CI} = \frac{L_1}{L_1 + L_1'} \quad (9)$$

and

$$k_{CO} = \frac{L_O}{L_O + L_O'} \quad (10)$$

This means that  $L_O$  avails a  $k_{CI}$  fraction of the energy that  $v_{LI}$  supplies, so  $L_1'$  reduces the effective *coupling factor* or *coupling coefficient*  $k_C$  to

$$k_C = k_{CI} k_L = \left( \frac{L_1}{L_1 + L_1'} \right) \sqrt{\frac{L_O}{L_1}} \quad (11)$$

This also means that  $L_O'$  is a load to  $L_O$ .

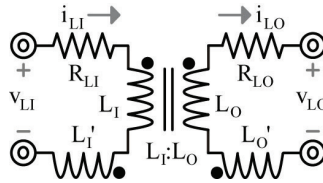


Fig. 3. Actual transformer.

Since separating the coils decreases the fraction of inductance that couples,  $L_1$  and  $L_O$  and their resulting  $k_C$  fall with increasing separation  $d_x$ . Misalignment between the coils also reduces  $k_C$ . Coupling also depends on the geometry of the coils, so variations in  $d_x$  manifest in  $k_C$  in a variety of ways.

$L_1$  and  $L_O$  are also resistive, and as a result, not lossless. So input and output resistances  $R_{LI}$  and  $R_{LO}$  further alter the  $k_C$  fraction that couples and reaches  $v_{LO}$ . Needless to say, better transformers *couple* more and *resist* less.

cases where  $i_{L(\text{MIN})}$  is not zero. Technically, PDCM is a special case of the more general DCM category. Although most often applied to zero cases,  $i_{L(\text{MIN})}$  in DCM can be any value.

**Example 3:** Determine  $t_E$ ,  $t_D$ , and  $\Delta i_L$  when  $v_E$  is 2 V,  $v_D$  is 1 V,  $i_{L(\text{MIN})}$  is zero,  $i_{L(\text{AVG})}$  is 25 mA,  $t_{\text{SW}}$  is 1  $\mu\text{s}$ , and  $L_X$  is 10  $\mu\text{H}$ .

**Solution:**

$d_E = 33\%$  and  $\Delta i_L = 66 \text{ mA}$  in CCM from previous example.

$$\begin{aligned} i_{L(\text{AVG})} &= 25 \text{ mA} < i_{L(\text{LIM})} + 0.5\Delta i_L \Big|_{\text{CCM}} \\ &= 0 + 0.5(66\text{m}) = 33 \text{ mA} \end{aligned}$$

$\therefore$  DCM

$$i_{L(\text{AVG})} = i_{L(\text{LIM})} + 0.5\Delta i_L \left( \frac{t_C}{t_{\text{SW}}} \right) = 0 + 0.5\Delta i_L \left( \frac{t_C}{t_{\text{SW}}} \right)$$

$$\Delta i_L = \left( \frac{v_E}{L_X} \right) t_E = \left( \frac{v_E}{L_X} \right) d_E t_C$$

$$\begin{aligned} \rightarrow t_C &= \sqrt{2i_{L(\text{AVG})} \left( \frac{L_X}{v_E} \right) \left( \frac{t_{\text{SW}}}{d_E} \right)} \\ &= \sqrt{2(25\text{m}) \left( \frac{10\mu}{2} \right) \left( \frac{1\mu}{0.33} \right)} = 870 \text{ ns} \end{aligned}$$

$$t_E = d_E t_C = (0.33)(870\text{n}) = 290 \text{ ns}$$

$$t_D = t_C - t_E = 870\text{n} - 290\text{n} = 580 \text{ ns}$$

$$\Delta i_L = \left( \frac{v_E}{L_X} \right) t_E = \left( \frac{2}{10\mu} \right) (290\text{n}) = 58 \text{ mA}$$

## 2.6. CMOS Implementations

Switches in a *complementary metal–oxide–semiconductor* (CMOS) implementation are *MOS field-effect transistors* (MOSFETs). Replacing

draw input power by connecting  $L_X$  across  $v_{IN}$  and ground. This way, with a positive  $v_E$  that is equal to  $v_{IN}$ ,  $L_X$  energizes.

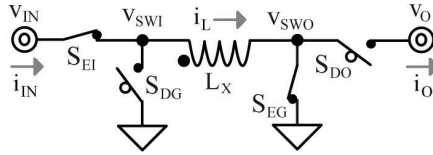


Fig. 9. Ideal buck-boost.

When done energizing,  $S_{EI}$  and  $S_{EG}$  open and drain switches  $S_{DG}$  and  $S_{DO}$  close to connect  $L_X$  to  $v_O$ .  $v_L$ 's polarity reverses this way to  $-v_O$ , so  $L_X$  drains into  $v_O$ .  $v_L$  in Fig. 5 therefore swings between  $+v_E$ 's  $v_{IN}$  and  $-v_D$ 's  $-v_O$  and  $i_L$  ramps up with  $+v_E$ 's  $v_{IN}$  and down with  $-v_D$ 's  $-v_O$ .

### B. Duty-Cycle Translation

In steady state,  $v_L$ 's average is zero, which is why engineers often say inductors are "dc shorts". The switching voltages  $v_{SWI}$  and  $v_{SWO}$  in Fig. 9 are therefore, on average, equal. Since  $v_{IN}$  connects to  $v_{SWI}$  a  $t_E$  fraction of  $t_C$  and  $v_O$  connects to  $v_{SWO}$  a  $t_D$  fraction of  $t_C$ , their averages are matching duty-cycled fractions of  $v_{IN}$  and  $v_O$ :

$$\begin{aligned} v_{SW(AVG)} &= v_{SWI(AVG)} = v_E \left( \frac{t_E}{t_C} \right) = v_{IN} d_E \\ &= v_{SWO(AVG)} = v_D \left( \frac{t_D}{t_C} \right) = v_O d_D = v_O (1 - d_E) \end{aligned} \quad (27)$$

This means that  $v_O$  is a duty-cycled scalar  $d_E/d_D$  of  $v_{IN}$ :

$$v_O = v_{IN} \left( \frac{d_E}{d_D} \right) = v_{IN} \left( \frac{d_E}{1 - d_E} \right). \quad (28)$$

And since  $d_D$  is  $1 - d_E$ ,  $d_E$  is a  $v_O$  fraction of  $v_{IN} + v_O$ :

$$d_E = \frac{v_D}{v_E + v_D} = \frac{v_O}{v_{IN} + v_O}. \quad (29)$$

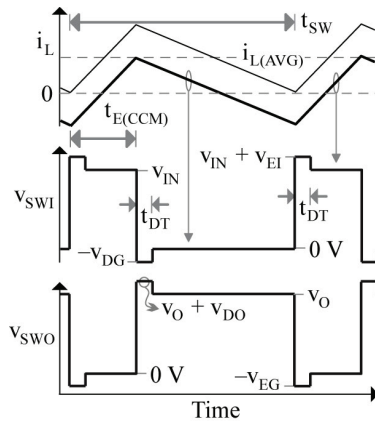


Fig. 16. Continuous conduction with reversing inductor current.

Since  $M_{DG}$ 's and  $M_{DO}$ 's body diodes are not bidirectional, reverse dead-time  $i_L$  does not flow through these diodes. Instead, negative  $i_L$  flows through  $M_{EG}$ 's and  $M_{EI}$ 's body diodes. So when  $M_{DG}$  and  $M_{DO}$  open before starting another  $t_{SW}$ ,  $v_{SWO}$  falls to  $-v_{EG}$  and  $v_{SW1}$  rises to  $v_{IN} + v_{EI}$  across  $t_{DT}$ , like Fig. 16 shows, instead of rising to  $v_O + v_{DO}$  and falling to  $-v_{DG}$  like a positive  $i_L$  induces.

The worst part about this is that  $L_X$  pulls power from  $v_O$  and returns it to  $v_{IN}$  when  $i_L$  reverses, which is the opposite of what a power supply should do. This is why designers often open  $M_{DG}$  and  $M_{DO}$  when  $i_L$  reaches zero, like diodes would. By forcing discontinuous conduction this way, the system does not burn Ohmic power to deliver and return energy that  $v_O$  does not receive.

#### D. Diode Conduction

$M_{DG}$ 's and  $M_{DO}$ 's body diodes conduct dead-time  $i_L$  like  $D_{DG}$  and  $D_{DO}$  in Fig. 10. In other words, the synchronous network operates like the asynchronous converter across  $t_{DT}$ 's. If MOSFET threshold voltages are lower than diode voltages,  $v_{SW1}$  falls below  $M_{DG}$ 's grounded drain and gate terminals until  $M_{DG}$ 's implicit diode action drops  $v_{GS}$  and conducts.  $v_{SWO}$  similarly climbs above  $M_{DO}$ 's  $v_O$ -supplied gate and drain terminals



until  $M_{DO}$ 's resulting diode connection drops  $v_{SG}$  and conducts. So  $M_{DG}$ 's and  $M_{DO}$ 's body diodes do not conduct into the substrate or  $M_{DO}$ 's body, which would otherwise inject noise power into the shared substrate.

When thresholds are higher than diode voltages and noise power is unacceptably high, designers connect Schottky diodes across  $M_{DG}$ 's and  $M_{DO}$ 's body diodes like Fig. 17 shows. This way, with the lower voltages that Schottkys require to conduct, the Schottkys conduct most of the dead-time current. Steering current away from the body diodes this way reduces the noise-producing current that would otherwise flow through the substrate.

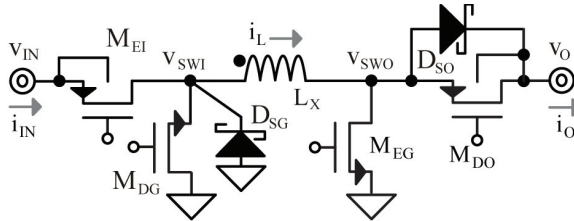


Fig. 17. Schottky-clamped synchronous buck-boost.

## 4. Buck

### 4.1. Ideal Buck

#### A. Power Stage

As the name implies, buck SLs *buck*  $v_{IN}$  to a lower  $v_O$ . Since  $v_{IN}$  is always greater than  $v_O$ ,  $v_{IN} - v_O$  can be the  $v_E$  that energizes  $L_X$ .  $v_{IN}$  energizes  $L_X$  into  $v_O$  directly this way. This is good because  $v_{IN}$  delivers energy with  $i_L$  into  $v_O$  that  $L_X$  does not need to carry and transfer. As a result,  $i_L$  peaks to a lower value than in the buck-boost. And with a lower  $i_L$ , series resistances burn less power, so  $P_O$  in a buck is usually a higher fraction of  $P_{IN}$  than  $P_O$  is in a buck-boost.

The switches that connect  $L_X$  to  $v_O$  in the buck-boost in Fig. 9 disappear in the buck of Fig. 18 because  $L_X$  both energizes and drains to  $v_O$ . Here, energize switch  $S_{EI}$  draws input power by connecting  $L_X$  across

$t_D$  and  $t_C$  are shorter and  $t_E$  is a larger fraction of  $t_C$ . In other words,  $d_E$  is higher than in the ideal boost.

As in the buck–boost,  $v_{SWO}$  swings between ground and  $v_O + v_{DO}$ , like Fig. 11 shows.  $v_{SWO}$  therefore connects to ground a  $t_E$  fraction of  $t_C$  and to  $v_O + v_{DO}$  a  $t_D$  fraction  $d_D'$ , so  $v_{IN}$  and  $v_{IN}'$ 's matching  $v_{SWO(AVG)}$  are

$$v_{IN} = v_{SWO(AVG)} = (0)d_E' + (v_O + v_{DO})d_D' = (v_O + v_{DO})(1 - d_E'). \quad (50)$$

Since  $d_D'$  is  $1 - d_E'$  and  $v_O - v_{IN}$  is less than  $v_O$ , the diode raises  $v_D$ 's  $v_O - v_{IN}$  in the numerator of  $d_E'$  by a larger fraction than in the denominator that  $v_E$ 's  $v_{IN}$  and  $v_D$ 's  $v_O - v_{IN}$  establish:

$$d_E' = \frac{v_D}{v_E + v_D} = \frac{v_O + v_{DG} - v_{IN}}{v_O + v_{DG}} > d_E. \quad (51)$$

So the effect of the diodes is to increase  $d_E$ .

**Example 13:** Determine  $d_E$  when  $v_{IN}$  is 1 V,  $v_O$  is 2 V, and  $D_{DO}$  drops 0.7 V.

**Solution:**

$$d_E' = \frac{v_O + v_{DG} - v_{IN}}{v_O + v_{DG}} = \frac{1 + 0.7}{2 + 0.7} = 63\%$$

**Note:**  $d_E'$  here is higher than  $d_E$  in the ideal example because  $D_{DO}$  increases  $L_X$ 's drain voltage. So  $t_D$  shortens and  $t_E$ 's fraction of  $t_C$ 's  $t_D + t_E$  increases.

### C. Conduction Modes

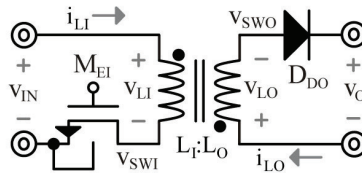
In static applications, the input is either a dc source or the output of a regulator that feeds a steady  $v_{IN}$ . Designers normally add capacitance to the output of regulators because controllers cannot respond instantaneously. So either way,  $v_{IN}$ 's equivalent  $C_{IN}$  is intentional and

fabrication lots, and temperature. So engineers often resort to empirical methods (via simulations or experiments) when choosing  $R_S$  and  $C_S$ . Dampers are usually preferable over clampers because  $R_S$  in clampers burns not only excess  $L_I$  energy but also core energy meant for  $v_O$ . Although less frequently included, a damper across  $S_{DO}$  similarly protects  $S_{DO}$  from the effects of remnant  $i_{L_O}$  in  $L_O$ .

## 6.2. Asynchronous Flyback

### A. Power Stage

In the asynchronous flyback,  $L_I$  energizes the core with a transistor and  $L_O$  drains the core with a diode. Since electrons are more mobile than holes, an NFET burns and requires less power than a PFET under equivalent gate-drive conditions. For maximum gate drive, the source of this NFET should connect to the lowest potential. This is why  $M_{EI}$  in Fig. 31 is the N-channel ground switch that energizes  $L_I$ . The source points to  $v_{IN}$ 's ground (away from the channel through which  $i_{L_I}$  flows) because N-channel sources output current. The P-type bulk also connects to  $v_{IN}$ 's ground to keep  $M_{EI}$ 's body diode from conducting when  $v_{L_I}$  "flies" high.



**Fig. 31.** Asynchronous flyback.

$M_{EI}$  energizes the core by feeding  $i_{L_I}$  into  $L_I$ 's dotted terminal.  $L_O$  must therefore drain  $i_{L_O}$  out of the opposite (non-dotted) terminal. This is why  $D_{DO}$  in Fig. 31 is the supply switch that drains  $i_{L_O}$  into  $v_O$ . Since  $D_{DO}$  blocks reverse current,  $v_{L_O}$  "flies" high when  $M_{EI}$  energizes  $L_I$ . Although connecting  $D_{DO}$  in  $v_O$ 's ground path also works, grounding  $L_O$  without a switch in series ties  $L_O$  to the least noisy terminal with lower resistance.