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# *Power Losses in Switched Inductors*

*Switched-inductor* (SL) power supplies are pervasive in electronic systems because they output a large fraction of the power they draw from their inputs. The main reason for this is the voltages that switches drop are a very small fraction of the output voltage. So the inductor current usually delivers a lot more power into the output than switches consume.

Still, the heat that burning power generates can compromise electronic performance and mechanical integrity. And losing battery energy or ambient power to the switched inductor reduces the charge life or functionality of a system. So understanding the nature, makeup, and sensitivity of these losses is important.

The most fundamental of these is *conduction power*. This is the power that components consume when they conduct inductor current. Series resistances, diodes, and transistors are to blame for this. Another loss is the power that gate drivers need to transition switches between states. Stray capacitances and large switches also leak power.

The operating mechanics of the switched inductor dictate how these components dissipate power. Quantifying losses, however, is not enough. Their significance ultimately rests on the applications they serve.

## **1. Power Conversion**

*Power-conversion efficiency*  $\eta_C$  is the fraction of *input power*  $P_{IN}$  that the *input*  $v_{IN}$  delivers to the *output*  $v_O$  in Fig. 1:

$$\eta_C \equiv \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_{LOSS}} = \frac{P_{IN} - P_{LOSS}}{P_{IN}} = 1 - \frac{P_{LOSS}}{P_{IN}} = 1 - \sigma_{LOSS}. \quad (1)$$

In addition to this *output power*  $P_O$ ,  $P_{IN}$  also supplies *power losses*  $P_{LOSS}$ . So  $P_O$  outputs the difference  $P_{IN} - P_{LOSS}$ , *fractional loss*  $\sigma_{LOSS}$  is the

from  $v_{IN}$  and ground and output drain switches  $S_{DG}$  and  $S_{DO}$  drain  $L_X$  into  $v_O$  in alternating phases. This way,  $v_{IN}$  produces an *inductor current*  $i_L$  that draws  $P_{IN}$  from  $v_{IN}$  and outputs  $P_O$  to  $v_O$ .

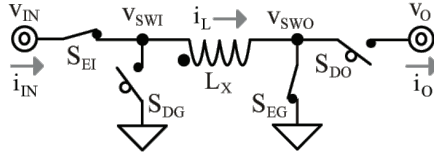


Fig. 6. Switched inductor.

$v_{IN}$  produces an *energize voltage*  $v_E$  that raises  $i_L$  across *energize time*  $t_E$  in Fig. 7.  $v_O$  similarly establishes an opposing *drain voltage*  $v_D$  that reduces  $i_L$  across *drain time*  $t_D$ .  $i_L$  rises and falls this way across  $t_C$  to produce a *inductor ripple current*  $\Delta i_L$  that repeats across cycles:

$$\Delta i_L = \left( \frac{v_E}{L_X} \right) t_E = \left( \frac{v_D}{L_X} \right) t_D. \quad (4)$$

Here, *energize* and *drain duty cycles*  $d_E$  and  $d_D$  refer to corresponding  $t_E$ 's and  $t_D$ 's fractions of  $t_C$ :  $t_E/t_C$  and  $t_D/t_C$ .

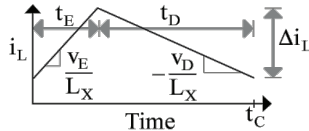


Fig. 7. Inductor current.

So  $t_E$  to  $t_D$ 's ratio follows  $d_E$  to  $d_D$ 's and matches  $v_D$  to  $v_E$ 's:

$$\frac{t_E}{t_D} = \frac{d_E}{d_D} = \frac{v_D}{v_E} = \frac{d_E}{1-d_E}. \quad (5)$$

Since  $t_D$  is  $t_C - t_E$  and  $d_D$  is  $1 - d_E$ ,  $d_E$  is  $v_D$ 's fraction of  $v_E$  and  $v_D$ :

$$d_E = \frac{v_D}{v_E + v_D}. \quad (6)$$

$d_E$  is therefore a function of the  $v_E$  and  $v_D$  that  $v_{IN}$  and  $v_O$  set.

Drain switches  $S_{DG}$  and  $S_{DO}$  open a  $t_{DT}$  before  $t_D$  ends, so  $D_{DG}$  and  $D_{DO}$  pull  $v_{SWI}$  a  $v_{DG}$  below ground and  $v_{SWO}$  a  $v_{DO}$  over  $v_O$ . And  $v_{SWI}$  climbs to  $v_{IN}$  and  $v_{SWO}$  falls to zero when energize switches  $S_{EI}$  and  $S_{EG}$  close at the beginning of  $t_E$ . This sequence repeats every  $t_{SW}$ .

### 3. Ohmic Loss

*Ohmic power*  $P_R$  refers to power that resistances in the switched inductor consume when conducting  $i_L$ . This is a loss because they burn  $v_{IN}$  power that  $v_O$  does not receive. The average power a device that conducts  $i_A$  and drops  $v_A$  consumes across time  $t_X$  is

$$P_{AX} \equiv P_{A(AVG)} \Big|_0^{t_X} = \frac{1}{t_X} \int_0^{t_X} P_A dt = \frac{1}{t_X} \int_0^{t_X} i_A v_A dt. \quad (13)$$

Since the voltage  $v_R$  across a resistor  $R_X$  that conducts  $i_X$  is  $i_X R_X$ ,  $R_X$  power  $P_R$ 's  $i_X v_R$  is  $i_X^2 R_X$ . When  $i_X$  ramps linearly across time  $t_X$  like Fig. 14 shows,  $P_R$  climbs quadratically with  $i_X$  and  $P_R$ 's average  $P_{RX}$  rises quadratically with  $i_X$ 's *root-mean-square* (RMS)  $i_{X(RMS)}$ :

$$P_{RX} = \frac{1}{t_X} \int_0^{t_X} i_X v_R dt = \left( \frac{1}{t_X} \int_0^{t_X} i_X^2 dt \right) R_X = i_{X(RMS)}^2 R_X. \quad (14)$$

This means that  $P_{RX}$ 's rise accelerates with  $i_X$ .

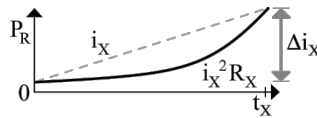


Fig. 14. Resistor power with ramp current.

### 3.1. Ohmic Power

#### A. Triangular Current

The *triangular current*  $i_\Delta$  in Fig. 15 ramps across  $t_X$  to  $\Delta i_\Delta$ . Squaring this  $i_\Delta$  and averaging  $i_\Delta^2$  across  $t_X$  reduces  $i_{\Delta(RMS)}$  to

$$i_{L(PK)} = \sqrt{2d_E t_{SW} \left( \frac{v_E}{L_X} \right) i_O}$$

$$= \sqrt{2(51\%)(1\mu) \left( \frac{4-2}{10\mu} \right) (10m)} = 45 \text{ mA}$$

$$P_{DT} \approx i_{L(PK)} v_{DG} \left( \frac{t_{DT}}{t_{SW}} \right) = (45m)(400m) \left( \frac{50n}{1\mu} \right) = 900 \text{ } \mu\text{W}$$

$$\sigma_{DT} = \frac{P_{DT}}{(i_O/d_{DO})d_{EI}v_{IN}} = \frac{900\mu}{(10m/1)(51\%)(4)} = 4.4\%$$

**Note:**  $P_{DT}$  is a higher fraction of  $P_{IN}$  in DCM than in CCM because  $P_{IN}$  scales down faster with  $i_O$  than  $P_{DT}$  with  $\sqrt{i_O}$ .

## 5. $i_{DS}$ - $v_{DS}$ Overlap Loss

$i_{DS}$ - $v_{DS}$  overlap power  $P_{IV}$  refers to the transitional power transistors consume when switching between on and off states.  $P_{IV}$  is essentially the power the *drain-source current*  $i_{DS}$  burns across the *drain-source voltage*  $v_{DS}$  drops when  $i_{DS}$  and  $v_{DS}$  transition. This loss hinges on the  $i_L$  that  $i_{DS}$  carries, the voltage that  $v_{DS}$  collapses, and their transition times.

Since  $i_{DS}$  scales with *gate-source voltage*  $v_{GS}$ , the aim of gate drivers is to transition gate voltages quickly. So they charge and discharge *gate-source* and *-drain oxide capacitances*  $C_{GS}$  and  $C_{GD}$  with low *pull-down/up N/P-type resistances*  $R_N$  and  $R_P$ . The resulting transitions should be shorter than dead times, so  $i_L$  is practically steady across these events.

### 5.1. Closing Switch

#### A. Power

When a switch is open,  $v_{GS}$  and  $i_{DS}$  are zero and  $v_{DS}$  is at a level  $v_{SW}$  that other components set. So when closing  $M_{SW}$  in Fig. 22,  $v_{GS}$  and later  $i_{DS}$  climb as  $R_P$  charges  $C_{GS}$  and  $C_{GD}$ .  $v_{DS}$  falls when  $i_{DS}$  is high enough to

$R_N = 20 \Omega$ ,  $v_{DD} = 4 \text{ V}$ ,  $v_{TH(O)} = 550 \text{ mV}$  from Example 10

$L_{CH} = L - 2L_{OL} = 250\text{n} - 2(30\text{n}) = 190 \text{ nm}$

$M_P$ 's  $v_{SD} = v_{DD} - v_{TH(C)}$

$$W_P = \frac{L_{CH}}{R_U K_P' \left[ v_{DD} - |V_{TP0}| - 0.5(v_{DD} - v_{TH(C)}) \right]}$$

$$= \frac{190\text{n}}{(100)(40\mu) \left[ 4 - 400\text{m} - 0.5(4 - 530\text{m}) \right]} = 26 \mu\text{m}$$

$M_N$ 's  $v_{DS} = v_{TH(O)}$

$$W_N = \frac{L_{CH}}{R_D K_N' (v_{DD} - V_{TN0} - 0.5v_{TH(O)})}$$

$$= \frac{190\text{n}}{(20)(200\mu) \left[ 4 - 400\text{m} - 0.5(550\text{m}) \right]} = 14 \mu\text{m}$$

## 6.2. Closing Switch

When closing  $M_{SW}$  in Fig. 28,  $M_P$  supplies the *gate current*  $i_G$  that  $C_{GB}$ ,  $C_{GS}$ , and  $C_{GD}$  need and the  $i_{ST}$  that  $M_N$  leaks.  $i_{ST}$  is low and short-lived (by design) because  $M_{SW}$ 's low  $v_{GS}$  suppresses  $M_N$ 's  $v_{DS}$  as  $v_I$ 's fall collapses  $M_N$ 's  $v_{GS}$ .  $i_G$  is much greater because  $M_P$ 's  $v_{SG}$  and  $v_{SD}$  are high across the time  $M_N$  leaks  $i_{ST}$ . So the *driver current*  $i_D$  that  $v_{DD}$  supplies is mostly the charge  $q_G$  that  $C_{GB}$ ,  $C_{GS}$ , and  $C_{GD}$  need to close  $M_{SW}$ .

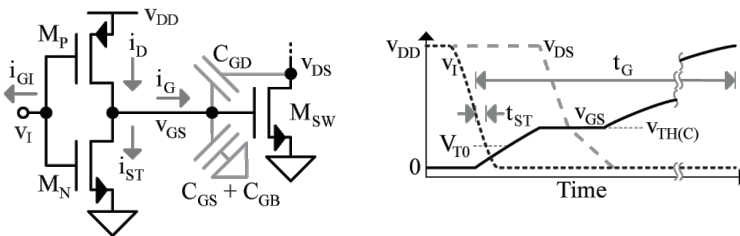


Fig. 28. Gate driver closing switch.

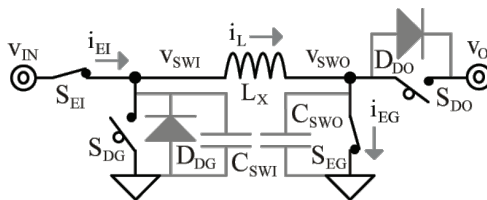


$$\begin{aligned}
 P_D &\approx V_{DD} \left( \frac{q_G + q_{GN} + q_{GP}}{t_{SW}} \right) \\
 &= 4 \left( \frac{400\text{p} + 85\text{f} + 160\text{f}}{1\mu} \right) = 1.6 \text{ mW} \\
 \sigma_D &= \frac{P_D}{(i_O/d_{DO})d_{EI}V_{IN}} = \frac{1.6\text{m}}{(250\text{m}/49\%)(1)(2)} = 0.2\%
 \end{aligned}$$

**Note:**  $q_G$  is usually much greater than  $q_{GI}$ . This  $P_D$ , which is 0.2% of  $P_{IN}$ , excludes the power  $M_{DO}$ 's driver consumes.

### 7. Leaks

MOS transistors also embody *source–* and *drain–body junction capacitances*  $C_{SB}$  and  $C_{DB}$ . The terminals that do not connect to the switching nodes connect to ground,  $v_{IN}$ , or  $v_O$ , which are nearly fixed. So  $C_{SB}$  and  $C_{DB}$  add *input and output switch-node capacitances*  $C_{SWI}$  and  $C_{SWO}$  that charge and discharge with  $v_{SWI}$  and  $v_{SWO}$  in Fig. 30. *Electrostatic-discharge protection* (ESD), pads, pins, and board connections also add capacitance to  $C_{SWI}$  and  $C_{SWO}$ .



**Fig. 30.** Switched inductor with parasitic diodes and capacitances.

Charging  $C_{SWI}$  and  $C_{SWO}$  requires energy that  $v_O$  unfortunately does not fully recovers. Power switches also leak current when they are off, especially when they are large and hot. Although these losses are usually low, they become increasingly larger fractions of  $P_{IN}$  when  $P_O$  fades.

$$W \equiv W_{CH}' = \sqrt{\frac{k_R}{k_G}} = \sqrt{\frac{79\mu}{7.6m}} = 100 \text{ mm}$$

$$R_{CH} = \frac{590\mu}{W_{CH}'} = 5.9 \text{ m}\Omega$$

$$P_{MOS} \approx 2\sqrt{k_R k_G} = 2\sqrt{(79\mu)(7.6m)} = 1.6 \text{ mW}$$

$$\sigma_{MOS} = \frac{P_{MOS}}{(i_O/d_{DO})d_{EI}v_{IN}} = \frac{1.6m}{(250m/32\%)(68\%)(2)} = 0.2\%$$

**Note:**  $P_{MOS}$ , which includes  $M_{DG}$ 's  $P_R$  and the driver's  $P_G$ , is much lower than  $P_R$  in Example 2 because  $R_{CH}$  is much lower.

### 8.3. Gate Driver

Similar transition times balance propagation delays and distribute switching losses across the switching period. This way, dead times and response time are consistent and peak transient power balances across switching events. Pull-up and -down resistances in the gate driver (which transistor  $W/L$ 's,  $K_N'$  and  $K_P'$ ,  $v_{GS}$  and  $v_{SG}$ , and  $V_{TN0}$  and  $V_{TP0}$  set) match opposing  $v_{SW}$  transition times  $t_{V(C)}$  and  $t_{V(O)}$  when  $R_P$ -to- $R_N$ 's ratio is

$$\begin{aligned} \frac{R_P}{R_N} &= \left(\frac{W_N}{W_P}\right) \left(\frac{L_P}{L_N}\right) \left(\frac{K_N'}{K_P'}\right) \left[ \frac{v_{DD} - V_{TN0} - 0.5v_{TH}}{v_{DD} - |V_{TP0}| - 0.5(v_{DD} - v_{TH})} \right] \\ &\equiv \left(\frac{v_{DD} - v_{TH(C)}}{v_{TH(O)}}\right) \left(\frac{C_{OL}v_{SW} + 0.25C_{CH}v_{TH(O)}}{C_{OL}v_{SW} + 0.25C_{CH}v_{TH(C)}}\right) \end{aligned} \quad (81)$$

Although not perfectly matched, these resistances produce similar  $i_{DS}$  transitions  $t_{I(C)}$  and  $t_{I(O)}$ . And since dead-time diodes set  $v_{DS}$  before and after switches close,  $v_{DS}$  swings the same  $v_{SW}$  when closing and opening. So excluding reverse recovery, the overlap power that switches consume when closing and opening reduces to

For this, the controller should adjust  $t_{sw}$  (not  $d_E$ ), which is a form of *frequency modulation* (FM). *Constant on-time control* and *pulse-FM* (PFM), for example, fix  $t_E$  and vary the frequency that  $L_X$  delivers energy packets. *Burst mode* is a variation that adjusts either the number of consecutive energy packets delivered between conduction gaps or the conduction gap between consecutive energy packets.

Figure 33 shows the efficiency of a photovoltaic battery-charging voltage regulator that adjusts the frequency of energy packets in discontinuous conduction.  $\eta_C$  is nearly constant at 95% when  $L_X$  is  $3 \times 3 \times 1.5 \text{ mm}^3$ .  $\eta_C$  is lower, but still constant when  $L_X$  is  $1.6 \times 0.8 \times 0.8 \text{ mm}^3$  because a smaller  $L_X$  is more resistive and therefore lossier.  $\eta_C$  drops when the *load power*  $P_{LD}$  that sets  $P_O$  nears zero because the controller consumes quiescent that does not scale with  $f_{sw}$  (or  $P_O$ ).

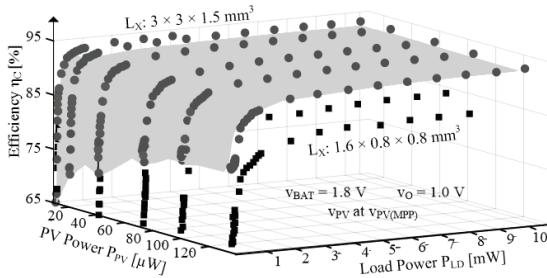


Fig. 33. Efficiency of frequency-modulated DCM system.

## 8.5. Power-Conversion Efficiency

### A. Loss Dominance

Power-conversion efficiency refers to the fraction of  $P_{IN}$  that  $P_O$  outputs.  $\eta_C$  is ultimately a reflection of fractional losses. So increasing  $\eta_C$  amounts to reducing  $\sigma_{LOSS}$ .

Ohmic, gate-charge, dead-time, overlap, and output power all scale with switching frequency when frequency-modulated in discontinuous conduction. So when very lightly loaded, the  $i_O$  that sets  $P_O$  is so low that