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Switched Inductors: Control Loops

Switched-inductor (SL) power supplies normally close feedback loops that sense the output, amplify the error, and adjust inductor current so the error is low. With this feedback action, they can feed any current the load or controller demands. This is how *voltage regulators*, *battery chargers*, and *light-emitting diode* (LED) *drivers* supply power.

Perhaps the most distinguishing feature in their implementations is how the error adjusts the inductor current. In this respect, although often described in unique and stand-alone terms, most switched-inductor power-supply systems evolve from two basic primitives. Variations on these then germinate features and restrictions that ultimately set them apart.

1. Primitives

1.1. PWM Loop

A. Comparator

A *comparator* compares two analog voltages and outputs a digital voltage to indicate which is higher. The *output* v_O reaches the *output high* V_{OH} in Fig. 1 when the *positive input* v_P surpasses the *negative input* v_N and the *output low* V_{OL} when v_N exceeds v_P. In CMOS implementations, V_{OH} and V_{OL} are usually the *positive* and *negative power supplies* v_{DD} and v_{SS}.

The *differential input voltage* v_{ID} is the difference between v_P and v_N. From this perspective, v_O reaches V_{OH} when v_{ID} is positive and V_{OL} when v_{ID} is negative. Comparators therefore dual as *polarity detectors*.

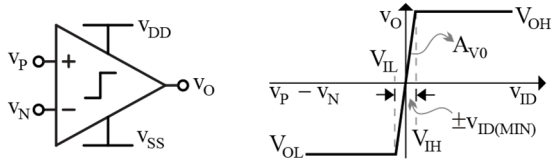

Fig. 1. Comparator.

Solution:

$$\Delta v_S = v_{S(HI)} - v_{S(LO)} = 500m - 200m = 300\ mV$$

$$v_I = v_{S(LO)} + \Delta v_S d_O = 200m + (300m)(45\%) = 340\ mV$$

$$v_I = v_{S(HI)} - \Delta v_S d_O = 500m - (300m)(45\%) = 360\ mV$$

$$d_{O(MIN)} = \frac{t_P}{t_{CLK}} = \frac{100n}{1\mu} = 10\%$$

C. PWM Loops

The *PWM voltage loop* in Fig. 8 is the classic *PWM voltage-mode regulator*. CP_{PWM} and v_S translate the *amplified error voltage* v_{EO} into the *energize duty-cycle command* d_E' that energizes the *switched inductor* L_X. f_{CLK} determines the *switching frequency* and *period* f_{SW} and t_{SW} of L_X.

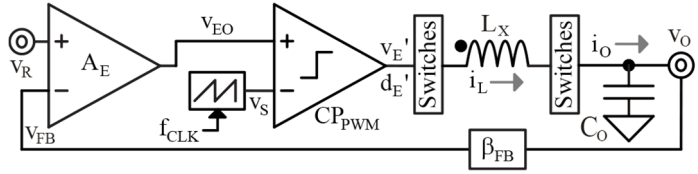

Fig. 8. PWM voltage loop.

The *feedback translation* β_{FB} scales v_O to the *feedback voltage* v_{FB} that the *error amplifier* A_E compares to the *reference voltage* v_R. So A_E outputs the v_{EO} that sets and adjusts d_E' so L_X's *inductor current* i_L supplies the *output current* i_O needed to keep the error low. This way, v_{FB} nears v_R and v_O is close to a reverse β_{FB} translation of v_R.

The *PWM current loop* in Fig. 9 is a direct translation of the voltage loop in Fig. 8. This loop senses and regulates i_L or i_O. So the error that feeds CP_{PWM} and adjusts d_E' is the *current-error voltage* v_{IO}.

The *current-feedback translation* β_{IFB} scales i_L or i_O to the *current-feedback voltage* v_{IFB} that the *current-error amplifier* A_{IE} compares to the *current-reference voltage* v_{IR}. A_{IE} outputs the v_{IO} that sets and adjusts d_E'

1.2. Hysteretic Loop

A. Hysteretic Comparator

The *hysteretic comparator* CP_{HYS} in Fig. 11 is a comparator that decouples and shifts v_{ID}'s *rising* and *falling trip points* $v_{T(HI)}$ and $v_{T(LO)}$. This way, v_O rises to V_{OH} after v_{ID} rises over $v_{T(HI)}$ and falls to V_{OL} after v_{ID} falls under $v_{T(LO)}$. But v_O does not trip when v_{ID} rises over $v_{T(LO)}$ or when v_{ID} falls below $v_{T(HI)}$. The difference between these trip-points is the *hysteresis* Δv_T.

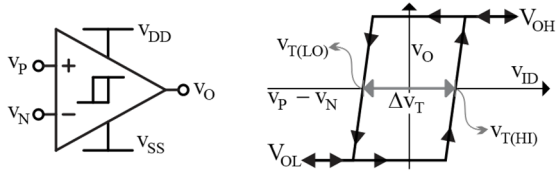

Fig. 11. Hysteretic comparator.

v_N's trip points oppose v_P's in v_{ID}. This is because v_O trips low when v_N rises $-v_{T(LO)}$ over v_P and trips high when v_N falls $-v_{T(HI)}$ below v_P. This is like saying v_N's $v_{T(HI)}$ and $v_{T(LO)}$ are v_P's $-v_{T(LO)}$ and $-v_{T(HI)}$.

B. Hysteretic Loops

The *hysteretic current loop* in Fig. 12 is a *relaxation oscillator* that centers on the hysteretic comparator and slewing action of i_L. β_{IFB} is usually a resistor that converts i_L to v_{IFB}. This way, v_{IFB} rises and falls with i_L.

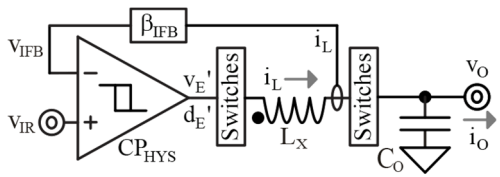

Fig. 12. Hysteretic current loop.

CP_{HYS} waits for the v_E the switcher impresses across L_X to slew i_L and v_{IFB} high to v_{IFB}'s $v_{T(HI)}$ in Fig. 13. When v_{IFB} overcomes $v_{T(HI)}$, CP_{HYS} trips v_E' low. This prompts the switcher to apply v_D across L_X, which slews i_L down. CP_{HYS} "relaxes" as i_L slews down, until v_{IFB} reaches v_{IFB}'s $v_{T(LO)}$. At this point, CP_{HYS} trips high and v_{IFB}'s $i_L\beta_{IFB}$ again climbs towards $v_{T(HI)}$.

$$\begin{aligned}\Sigma v_{ID} &= v_{EO} - v_{IFB} - v_S = (v_R - v_{FB})A_E - v_{IFB} - v_S\big|_{A_E \equiv 1} \\ &= v_R - v_{FB} - v_{IFB} - v_S = v_R + (-v_S) - v_{FB} - v_{IFB}\end{aligned} . \tag{34}$$

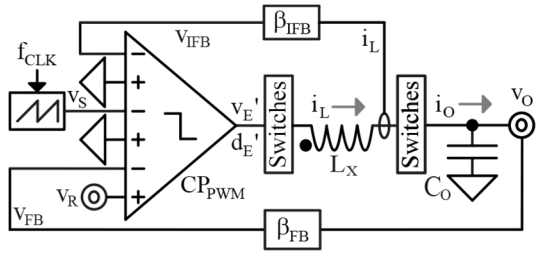

Fig. 22. Doubly-contracted PWM current-mode voltage loop.

This is like subtracting v_{FB} and v_{IFB} from v_R and $-v_S$. With v_S inverted this way, Σv_{ID} adds two v_P's and two v_N's like CP_{PWM} in Fig. 23. Either way, incorporating A_E and A_{IE} into CP_{PWM} is a *double contraction*.

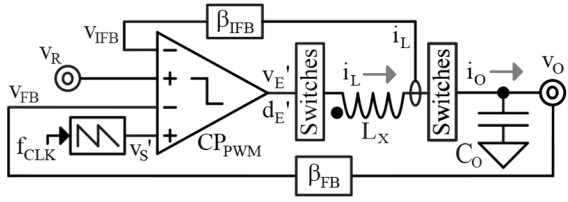

Fig. 23. Compact PWM current-mode voltage loop.

These double contractions are stable without z_{DO} when the *capacitor pole* p_C that C_O produces reduces A_{LG} to f_{0dB} at or below the *current loop's bandwidth* p_{IBW} that the *current loop's unity-gain frequency* f_{I0dB} sets. It is also stable when the roles of p_C and p_{IBW} reverse. p_C and p_{IBW} can also precede f_{0dB} when z_C reverses p_C at or below f_{0dB}. With z_{DO}, stable operating conditions are more elusive.

D. Offsets

The v_{IOS} needed to set d_E' is a d_E' fraction of Δv_S over $v_{S(LO)}$. Since this v_{IOS} is a v_P in Σv_{ID} and v_{IR} minus v_{IFB} generates v_{IOS}, v_{IFB} is v_{IOS} below v_{IR}. v_{FB} in the PWM voltage loop is similarly v_{IOS} below v_R:

$$v_{IOS} = v_{S(LO)} + \Delta v_S d_E' . \tag{35}$$

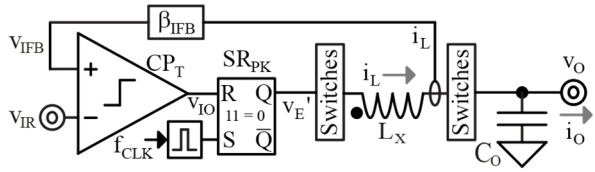

Fig. 37. Peak current loop.

t_R^+ is also the same. When v_{IR} rises suddenly, v_{IR} surpasses v_{IFB}, so v_{IO} falls and stays low. This raises and keeps v_E' high because, once f_{CLK} sets v_E', subsequent lows keep v_E' high. So i_L rises uninterruptedly across t_R^+.

t_R^-, however, is shorter. When v_{IR} falls suddenly, v_{IR} falls below v_{IFB}, so v_{IO} rises and stays high. This keeps v_E' low because the *peak flip flop* SR_{PK} is reset-dominant. This way, i_L falls uninterruptedly across t_R^-.

The *valley current loop* in Fig. 38 is the peak's complement. CP_T starts t_E when v_{IFB} falls below v_{IR}, v_{IFB} rises until f_{CLK} ends t_E, and v_E' stays low and high with v_{IO} across t_R's. So v_{IR} sets $v_{IFB(LO)}$, t_{CLK} fixes t_{SW}, and i_L rises and falls across t_R^+ and t_R^- without interruptions.

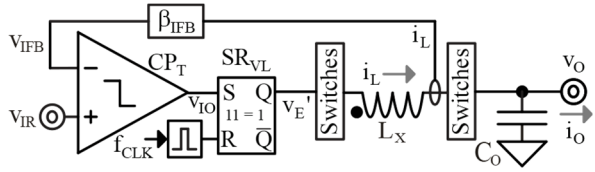

Fig. 38. Valley current loop.

B. Sub-Harmonic Oscillation

v_{IN} noise can change the di_L/dt that projects i_L across $\Delta v_{IFB}/\beta_{IFB}$, which can alter t_E or t_D. A temporary rise in v_E's v_{IN}, for example, raises di_L^+/dt in Fig. 39. So i_L reaches v_{IR}'/β_{IFB} sooner, falls across a longer t_D, and reaches di_{L0} below the nominal $i_{L(LO)}$.

di_{L0} extends the next t_E that di_L^+/dt projects. This shortens t_D because t_{SW} is constant. So di_L^-/dt projects i_L above the nominal $i_{L(LO)}$. Since d_E/d_D is v_D/v_E, the new imbalance di_{L1} is an inverting d_E/d_D translation of di_{L0}:

Slope compensation adds another *offset* v_{SOS}. v_S subtracts a d_E fraction of Δv_S from $v_{S(HI)}$ or adds a d_E fraction of Δv_S over $v_{S(LO)}$. So in all, v_{IOS} is

$$v_{IOS} = \frac{\Delta v_{IFB}}{2} - v_{IOS}{}^{+} + v_{SOS} = \frac{\Delta v_{IFB}}{2} - v_{IOS}{}^{+} \pm \left(v_{S(LO/HI)} \pm \Delta v_S d_E' \right). \quad (63)$$

Example 12:Determine $v_{S(HI)}$, Δv_{IFB}, v_{EO}, and v_{FB} for the peak current-mode voltage loop when v_R is 1.2 V, A_E is 10 V/V, β_{IFB} is 1 Ω, t_{CLK} is 1 µs, t_P is 100 ns, t_{SR} is 10 ns, $v_{S(LO)}$ is 200 mV, v_E is 2.2 V, v_D is 1.8 V, L_X is 10 µH, and $i_{L(AVG)}$ is 100–500 mA.

Solution:

$$\Delta v_S = t_{CLK}\left(\frac{dv_{IFB}}{dt}\right) \equiv t_{CLK}\left(\frac{0.5 v_D}{L_X}\right) = 90 \text{ mV}$$

$$v_{S(HI)} = v_{S(LO)} + \Delta v_S = 200\text{m} + 90\text{m} = 290 \text{ mV}$$

$$d_E = \frac{v_D}{v_E + v_D} = \frac{1.8}{2.2 + 1.8} = 45\%$$

$$t_E = t_{CLK} d_E = (1\mu)(45\%) = 450 \text{ ns}$$

$$\Delta v_{IFB} = t_E\left(\frac{v_E}{L_X}\right)\beta_{IFB} = (450\text{n})\left(\frac{2.2}{10\mu}\right)(1) = 99 \text{ mV}$$

$$t_P' = t_P + t_{SR} = 100\text{n} + 10\text{n} = 110 \text{ ns}$$

$$v_{IOS} = \frac{\Delta v_{IFB}}{2} - t_P'\left(\frac{v_E}{L_X}\right)\beta_{IFB} + v_{S(LO)} + d_E \Delta v_S$$

$$= \frac{99\text{m}}{2} - (110\text{n})\left(\frac{2.2}{10\mu}\right)(1) + 200\text{m} + (45\%)(90\text{m})$$

$$= 270 \text{ mV}$$

$$v_{EO} = i_{L(AVG)}\beta_{IFB} + v_{IOS} = i_{L(AVG)} + 270 \text{ mV} = 570 \pm 200 \text{ mV}$$

$$v_{FB} = v_R - \frac{v_{EO}}{A_E} = 1.2 - \frac{v_{EO}}{10} = 1.14 \text{ V} \pm 20 \text{ mV}$$

$$\therefore \quad \Delta v_{FB} \approx \Delta v_T + t_P \left(\frac{v_E + v_D}{R_F C_F} \right) \beta_{FB} = 41 \text{ mV}$$

$$= \Delta v_T + \frac{(100n)(2.2+1.8)(66\%)}{(800k)(20p)} \quad \rightarrow \quad \Delta v_T = 24 \text{ mV}$$

$$\Delta v_F = \frac{\Delta v_{FB}}{\beta_{FB}} = \frac{41m}{66\%} = 62 \text{ mV}$$

$$t_E = d_E t_{SW} = \left(\frac{v_D}{v_E + v_D} \right) t_{SW} = \left(\frac{1.8}{2.2+1.8} \right) (1\mu) = 450 \text{ ns}$$

$$\Delta v_O \approx \frac{v_E {t_E}^2 + v_D {t_D}^2}{8 L_X C_O} \approx \frac{v_E {t_E}^2 + v_D \left(t_{SW} - t_E \right)^2}{8 L_X C_O}$$

$$= \frac{(2.2)(450n)^2 + (1.8)(1\mu - 450n)^2}{8(10\mu)(5\mu)} = 2.5 \text{ mV}$$

Note: Δv_O is much lower than Δv_F.

D. Voltage-Mode Voltage Loop

The *voltage-mode voltage-looped buck* in Fig. 46 uses the filtered buck like a current loop. This way, β_{FB2} scales v_O to v_{FB2}, A_{E2} compares v_{FB2} to v_R, and the filtered buck translates v_{EO2} to $i_{L(AVG)}$. So v_{EO2} adjusts the $i_{L(AVG)}$ that sets i_O so v_{FB2} and v_O near v_R and v_R/β_{FB2}.

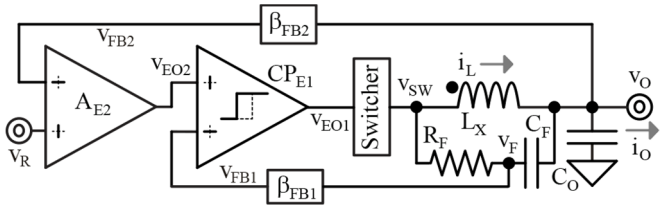

Fig. 46. Voltage-mode voltage-looped buck.

v_{FB2} and v_{EO2} are steady because C_O suppresses v_O's ripple. CP_{E1}, however, needs this v_{EO2} to carry a β_{FB1} translation of $v_{F(AVG)}$. v_R minus