Switched Inductors:

Building Blocks

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Contents

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Switched-inductor (SL) power supplies draw and deliver power. They are *regulators* when *feedback controllers* switch them so their outputs follow a target. *Voltage regulators* regulate voltage, *battery chargers* and *light-emitting diode* (LED) *drivers* regulate current, *battery-charging voltage regulators* regulate both, and *energy harvesters* regulate power.

Good power supplies are *efficient* and *accurate*. Efficient supplies lose a small fraction of the power they draw. And accurate supplies deliver the rest with a voltage or current that is very close to a target. Supplying power with a preset voltage or current like this is a form of *power conditioning*.

Power conditioning requires several actions. Some of these are analog in nature, others are digital, and those in between are mixed-mode. The building blocks that power supplies use reflect this diversity.

1. Current Sensors

1.1. Series Resistance

A. Sense Resistor

Inserting a *series resistor* R_S into the conduction path is one way of sensing current. R_S in Fig. 1 can be in series with the *switched inductor* L_X, the *output* v_O, or the *load* Z_{LD}. In all cases, the *current-feedback translation* β_{IFB} that senses v_O's *output current* i_O or L_X's *inductor current* i_L is R_S:

$$\beta_{IFB} \equiv \frac{v_{IFB}}{i_{L/O}} = \frac{i_{L/O} R_S}{i_{L/O}} = R_S \,. \tag{1}$$

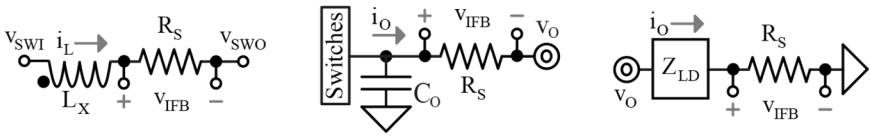

Fig. 1. Sense resistor.

average v_{SW}'s and extract R_L's dc voltage. A tuned bypass filter can extract R_L's dc and ac voltages, but with a v_{IFB} that swings with one of the v_{SW}'s. This is not a problem for bucks and boosts because they only have one v_{SW}, which the filter can average. This filter can also amplify R_L's ac voltage, but only after L_X overcomes R_L and C_F shorts.

R_S, R_{DS}, and R_L all vary with temperature and fabrication runs. Sense FETs are less sensitive because they track the switches they sense. But since they are much smaller, mismatches offset their outputs. Their translations are also nonlinear. A feedback loop can fix this, but by slowing the response. Although not always, basic sense FETs often offer more favorable tradeoffs than looped FETs and series resistances. Table I summarizes some of these points.

Table I. Current Feedback Translations

	Series Resistances					**Sense FETs**	
	R_S	**R_{DS}**	**Filtered R_L**			**Basic**	**Looped**
			Low Pass	**Tuned**	**Untuned**		
Input	$i_{O/L}$	$i_{O/L(E/D)}$	$i_{L(DC)}$	i_L	$i_{L(DC/AC)}$	$i_{O/L(E/D)}$	
Gain	R_S	R_{DS}	R_L	R_L	$\frac{L_X}{R_F C_F}$	$\frac{R_{IFB}}{A_I}$	
Power	$P_R + P_Q$	P_Q	P_Q	P_Q	P_Q	P_Q	
Sensitivity	T_J & Fabrication Runs $R_L \propto f_O$					Mismatch	
						Nonlinear	Linear

2. Voltage Sensors

2.1. Voltage Divider

v_O is typically over the *bandgap voltage* V_{BG} or sub-V_{BG} that sets the *reference voltage* v_R. So in most cases, the *feedback translation* β_{FB} attenuates v_O to the *feedback voltage* v_{FB} that the *error amp* A_E compares to v_R. This is why v_R is normally 1.2 V or lower and β_{FB} is a fraction.

$$\Delta PM = \tan^{-1}\frac{f_{0dB}}{z_{FB}} - \tan^{-1}\frac{f_{0dB}}{p_{FB}}. \qquad (22)$$

Example 5: Determine C_F and ΔPM for Example 4 when f_{0dB} is 100 kHz.

Solution:

R_{FB1} = 168 kΩ and R_{FB2} = 232 kΩ from Example 4

$$z_{FB} = \frac{1}{2\pi R_{FB1} C_F} = \frac{1}{2\pi(168k)C_F} = \frac{950n}{C_F}$$

$$p_{FB} = \frac{1}{2\pi\left(R_{FB1} \,||\, R_{FB2}\right)C_F} = \frac{1}{2\pi\left(168k \,||\, 232k\right)C_F} = \frac{1.6\mu}{C_F}$$

$$\frac{p_{FB}}{f_{0dB}} = \frac{1.6\mu}{(100k)C_F} \equiv \frac{f_{0dB}}{z_{FB}} = \frac{(100k)C_F}{950n}$$

$\therefore$ C_F = 12 pF $\rightarrow$ z_{FB} = 79 kHz and p_{FB} = 130 kHz

$$\Delta PM = \tan^{-1}\frac{f_{0dB}}{z_{FB}} - \tan^{-1}\frac{f_{0dB}}{p_{FB}}$$

$$= \tan^{-1}\frac{100k}{79k} - \tan^{-1}\frac{100k}{130k} = 14°$$

2.3. Voltage-Dividing Error Amplifier

When the feedback loop includes A_E, integrating β_{FB} into A_E's stabilizer can save power, components, and area. The *voltage-dividing error amplifier* in Fig. 11, for example, integrates the voltage divider into the feedback network of an *inverting op amp*. R_{FB1} and R_{FB2} translate v_O to v_{FB} and A_V, Z_{F1}, and Z_{F2} with R_{FB1} set A_E's gain and stabilizing response.

Z_{F1} and Z_{F2} are typically capacitors C_{F1} and C_{F2} with, on occasion, series resistors R_{F1} and R_{F2}. This way, Z_{F1} and Z_{F2} open at low frequency. So β_{FB} translates v_O to v_{FB} with R_{FB1} and R_{FB2} and A_E's *low-frequency gain* A_{E0} amplifies v_R and v_{FB}'s error with A_{V0}.

self-loading (k_{SL}) is negligible. $N(1 + f_o)/(1 + 3.6)$ when f_o is 3.6 nears a more optimal N_0 because k_{SL} is more realistic near one.

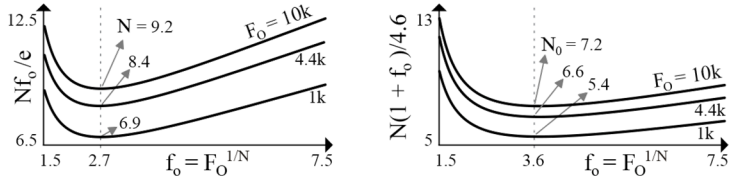

Fig. 19. Optimal gate-driver setting for minimum delay.

M_N in K_1 pulls v_{O1} low when i_N overcomes i_P, after v_{GS} reaches v_T. As v_{GS} rises over v_T and v_{O1} falls across $\Delta v_{O(MAX)}$, M_N enters and remains in triode. M_P is similarly in triode as v_{SG} climbs over v_T and v_O rises. When strengths match, R_{D1} is roughly M_N's triode resistance when v_{GS} nears v_T:

$$R_{D1} \approx R_{N1}\Big|_{\substack{v_{GS}>V_{TN0}\\ v_{DS}<v_{DS(SAT)}}} \approx \frac{L_{N1} - 2L_{OL}}{W_{N1}K_N'\left(v_T - V_{TN0}\right)}, \tag{33}$$

where L_{OL} is *overlap length*. C_{GI} is roughly the *channel capacitance* C_{CH1} that W's and L's set across the *oxide capacitance* C_{OX}" (per unit area):

$$C_{GI} \approx C_{CH1} = C_{CHN1} + C_{CHP1} \approx \left(W_{N1}L_{N1} + W_{P1}L_{P1}\right)C_{OX}''. \tag{34}$$

Example 7: Determine N and t_P with the inverter from Example 6 when L_{MIN} is 250 nm, L_{OL} is 30 nm, C_{OX}" is 6.9 fF/μm^2, and the load is a 100-mm wide, 250-nm long NFET.

Solution:

W_{N1} = 3 μm and $W_{P1} = 6.7W_{N1}$ = 20 μm from Example 6

$L_{N1} \equiv L_{P1} \equiv L_{MIN}$ = 250 nm

$C_{GI} = C_{GN} + C_{GP} = C_{GN} + 6.7C_{GN} = 7.7C_{GN}$

$$F_O = \frac{C_{GO}}{C_{GI}} = \frac{W_{GO}}{7.7W_{GN}} = \frac{100\text{m}}{7.7(3\mu)} = 4.4\text{k}$$

$$F_O = f_o^{N_0} \equiv 3.6^{N_0} = 4.4\text{k} \quad \therefore \quad N \geq N_0 = 6.6 \;\rightarrow\; N \equiv 7 \text{ Stages}$$

same time. Consider gate command v_G' and *gate voltages* v_G and v_{GX} in Fig. 21, for example. v_G rises a t_{DT} after adjacent v_{GX} falls, even when v_G' commands a high before v_{GX} falls.

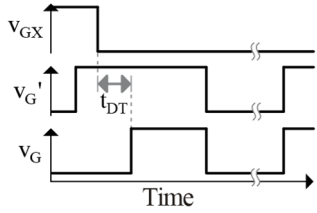

Fig. 21. Dead-time response.

t_{DT} only applies to closing events, when burning unnecessary power is possible. Opening switches is inherently safe because it stops current flow. This is why v_G falls with v_G' without delay in Fig. 21.

t_{DT} should delay turn-on commands only when adjacent commands are high, when shorting events are possible. Whenever safe, reducing delays helps the system respond and recover more quickly. This is why v_G in Fig. 21 rises with v_G' without delay the second time v_G' transitions high.

To assert these states, *dead-time circuits* should sense, delay, and compare neighboring commands with v_G'. R's and C's in Fig. 22, for example, sense and delay neighboring v_G's. And NOR and NAND gates compare these delayed signals with v_G' to determine v_G. R's and C's or inverter chains can sense and delay neighboring v_G's.

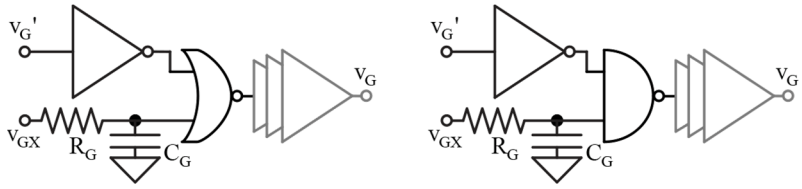

Fig. 22. Active-high and -low dead-time circuits.

The NOR gate outputs an active-high command when v_G' is high after neighboring v_G's fall. The NAND gate outputs an active-low command

$$v_{S(HI)} = v_T + \left(\frac{I_S}{C_S}\right) t_P{}^+ = v_T + \left(\frac{1.7\mu}{5p}\right)(100n) \equiv 300 \text{ mV}$$

$$\therefore \quad v_T = 270 \text{ mV}$$

5.3. One-Shot Oscillator

One-shot oscillators are *pulse generators*. But more specifically, they are interruptible relaxation oscillators. They pulse once when pulsed and pulse continuously when kept enabled.

Like *ring oscillators*, they usually close inverting feedback loops that internal components delay. In the case of Fig. 29, CP_R, the flip flop, and M_R close the loop and I_S and C_S delay it. v_O pulses each time v_I pulse-sets the flip flop and oscillates between states when v_I stays high.

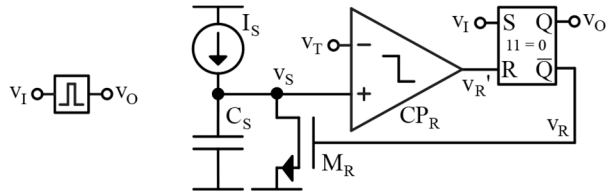

Fig. 29. One-shot oscillator.

Raising v_I sets v_O and opens M_R to start a pulse. I_S charges C_S across the pulse until M_R resets v_S. The *pulse width* t_{PW} is the time C_S, CP_R, and the reset-dominant flip flop need to ramp v_S to v_T, trip, and reset:

$$t_{PW} = \left(\frac{C_S}{I_S}\right)\left(v_{S(HI)} - v_{S(LO)}\right) = \left(\frac{C_S}{I_S}\right)\left(v_T - v_{S(LO)}\right) + t_P{}^+ + t_{SR}{}^+ . \qquad (48)$$

So across this t_{PW}, I_S charges C_S over v_T across $t_P{}^+$ and $t_{SR}{}^+$:

$$v_{S(HI)} = v_T + \left(\frac{I_S}{C_S}\right)\left(t_P{}^+ + t_{SR}{}^+\right). \qquad (49)$$

Keeping v_I high sets another pulse when the reset command v_R' falls. This happens after v_S falls below v_T. The time between pulses t_{OFF} is the

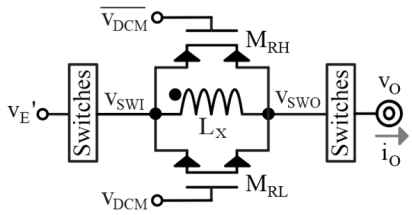

Fig. 34. Ring suppressor.

As R_L dampens oscillations, v_{SWI} and v_{SWO} approach one another until v_L is zero. Since bucks and boosts exclude input or output switches, v_{SW} approaches v_O in bucks and v_{IN} in boosts. The C_{SW} that sets the *LC time constant* τ_{LC} in buck–boosts is the series combination of C_{SWI} and C_{SWO}.

These oscillations can last several cycles. This is unfortunate because the *electromagnetic interference* (EMI) i_L generates can alter the feedback action that sets v_O or i_O. The purpose of $M_{RL/H}$ is to suppress this "ringing".

The *ring suppressor* is a resistor that the ZCD invokes when L_X enters DCM. This R_R should burn E_{LC} before L_X receives it. Since C_{SW} and L_X exchange E_{LC} every quarter *LC period* t_{LC}, t_{RC} should be less than 25%t_{LC}:

$$t_S = t_{RC} \approx 2.3\tau_{RC} = 2.3R_R C_{SW} < \frac{t_{LC}}{4} = \frac{2\pi\tau_{LC}}{4} = \frac{2\pi/4}{\sqrt{L_X C_{SW}}}, \qquad (54)$$

where *suppression time* t_S is roughly the t_{RC} needed to collapse 90% of v_L.

Low- and high-side switches can realize this R_R. A PFET M_{RH} may be sufficient when v_O is high and an NFET M_{RL} when v_{IN} exceeds v_O and v_O is low. Both may be necessary when v_{IN} is not much greater than a low v_O. Regardless, these FETs are often mostly in triode when they collapse v_L.

Example 16:Determine W_R when v_O for a buck is 1.8 V, L_X is 10 µH, C_{SW} is 5 pF, W_{MIN} is 3 µm, L_R is 250 nm, L_{OL} is 30 nm, K_P' is 40 µA/V^2, and V_{TP0} is –700 mV.

Solution:

$$L_{CH} = L_R - 2L_{OL} = 250n - 2(30n) = 190 \text{ nm}$$

efficient than adding resistance. This resistance, however, varies widely with temperature and fabrication runs. Sense transistors often offer more favorable tradeoffs in this respect. Their weakness is mismatch.

Voltage dividers sense and translate voltages well because resistors usually match well. Paralleling a capacitor across the top resistor is an easy way of inserting a phase-saving zero–pole pair. Combining the voltage divider with the stabilizing error amplifier is also possible.

Amplifiers and comparators compare analog inputs and output a digital output that indicates which is higher. Comparators are basically amplifiers without stabilizing features. Adding flip flops or positive feedback establishes hysteresis. And paralleling transconductors adds inputs so the output trips with the polarity of their sum.

Constant-time loops rely on timing blocks to operate. Capacitors are essential here. In sawtooth generators, current into a capacitor ramps a voltage that a flip flop resets. Sawtooth and one-shot oscillators ramp a voltage that a comparator resets. And a flip flop in the one shot can interrupt the oscillations to pulse once or any number of times.

Digital blocks control switching events. SR flip flops use digital gates and positive feedback to decouple on–off commands. Inverter chains with increasingly larger stages drive large power switches. And dead-time logic keeps adjacent power switches from shorting their inputs.

Switch blocks help manage switching events. Supply-sensing comparators are useful in this respect. They help zero-current detectors invoke DCM operation and switched diodes behave like ideal diodes. They can also trigger the ring suppressor, which subdues DCM oscillations.

The starter is also important. It keeps initial shutdown conditions from spiking i_L. Current and duty-cycle limiters are useful guardrails during