Errata for *Analog IC Design with Low-Dropout Regulators*

Prof. Gabriel A. Rincón-Mora, Ph.D.

Chapter 2

Page 69: "...the MOSFET enjoys the benefit of true symmetric performance..."

Chapter 3

Equation 3.4: \( G_{M,LF} \bigg|_{v_{out}=0} \approx \frac{i_{out}}{v_{in}} = \frac{v_{gs} g_m}{v_{gs} + v_R} = \frac{v_{gs} g_m}{v_{gs} + R \left(v_{gs} g_m\right)} = \frac{g_m}{1 + R g_m} \leq g_m \)

Equation 3.5: \( G_{M,LF} \bigg|_{v_{out}=0} \approx \frac{i_{out}}{v_{in}} = \frac{v_{gs} g_m - v_R g_{mb}}{v_{gs} + v_R} = \frac{g_m}{1 + (g_m + g_{mb}) R} \leq g_m \)

Equation 3.6: \( G_{M,LF} \bigg|_{v_{out}=0} \approx \frac{i_{out}}{v_{in}} = \frac{v_{gs} g_m}{v_{gs} + v_R} = \frac{v_{gs} g_m}{v_{gs} + R \left[v_{gs} g_m \left(1 + \frac{1}{\beta}\right)\right]} = \frac{g_m}{1 + R g_m} \leq g_m \)

Equation on page 89: \( \left( \frac{R}{sC} \right) = \frac{R}{1 + sRC} = \frac{R}{1 + \frac{s}{2\pi p}} \)

Equation 3.20:

\[
G_M = \frac{g_m}{1 + g_m \left( \frac{1}{sC_{PAR}} \right)} = \frac{g_m}{1 + g_m \left( \frac{R}{1 + sRC_{PAR}} \right)} = \frac{g_m \left(1 + sRC_{PAR}\right)}{\left[1 + g_m R \left(1 + \frac{sRC_{PAR}}{1 + g_m R}\right)\right]} \]

\[
= \frac{G_{M,LF} \left(1 + \frac{s}{2\pi \xi} \right)}{\left[1 + \frac{s}{2\pi \xi} \left(\frac{G_{M,LF}}{g_m}\right)\right]} = \frac{G_{M,LF} \left(1 + \frac{s}{2\pi p} \right)}{\left[1 + \frac{s}{2\pi \xi} \left(\frac{G_{M,LF}}{g_m}\right)\right]} \]
Figure 3.14:

- Assume Ideal Current Sources ($g_m = 0$)
- Small-Signal Variations

Figure 3.22:

Equation 3.78:
Since $Q_{IN} - Q_{O}$ mirrors $i_{gm.IN}$,

$$i_{b.CO} = \frac{i_{gm.IN}}{1 + \beta} \quad \text{and} \quad R_{IN} = \left( \frac{1}{g_{m.CIN}} + \frac{1}{g_{m.M}} \right) \parallel R_{IN.CO} = \frac{2}{g_m} \left( \frac{2}{g_m} (1 + \beta) \right) = \frac{2}{g_m}$$

Equation 3.81:

$$A_{I,LF} = \left. \frac{i_{Load}}{i_s} \right|_{\text{in}} = \left. \left( \frac{V_{in}}{i_s} \right) \left( \frac{V_{b.M}}{V_{in}} \right) \left( \frac{i_{gm.M}}{i_{gm.M}} \right) \left( \frac{V_{c.CO}}{i_{gm.CO}} \right) \left( \frac{i_{gm.CO}}{i_{gm.CO}} \right) \left( \frac{V_{out}}{V_{out}} \right) \right|_{\text{out}}$$

$$= \left( R_S \parallel R_{IN} \right) \left[ \frac{1}{g_{m.M}} \right] \left[ \frac{r_{e.CO} + R_{Load}}{1 + g_{m.CO}r_{e.CO}} \right] \left( g_{m.CO} \parallel R_{OUT} \parallel R_{Load} \right) \left( \frac{1}{R_{Load}} \right)$$

$$= \left( R_S \parallel R_{IN} \right) \left( \frac{1}{2} \right) \left( -g_{m.M} \right) \left( \frac{1}{g_{m.CO}} \right) \left( g_{m.CO} \right) \left( R_{OUT} \parallel R_{Load} \right) \left( \frac{1}{R_{Load}} \right)$$

$$= \left( \frac{2}{g_{m.M}} \right) \left( \frac{1}{2} \right) \left( -g_{m.M} \right) \left( \frac{1}{g_{m.CO}} \right) \left( g_{m.CO} \right) (1) = -1$$
Page 153, 2nd paragraph, line 14: “…to iO (i.e., approximately $g_m$) and iO to $v_{FB}$ (i.e., roughly R), respectively.”

Equation 4.15: 

$$A_{G,CL} = \frac{iO}{v_1} = \frac{A_{G,OL}}{1 + A_{G,OL} \beta_{FB}} = \frac{g_m}{1 + g_m R} = \frac{1}{R}$$
Page 168, 2nd paragraph, line 6: “…where the output voltage is zero, which means $i_o$ or $v_n/(r_i || R)$ is $v_c g_m(r_\pi || R)/r_o$ or approximately $g_m$."

Page 168, 3rd paragraph, line 12: “…current gain $A_{OL}$ is $i_o/i_c$, where $i_o$ is $M_C$’s gate voltage $v_{gC}$ (or approximately, $i_{ro1}AV$) into source-degenerated transconductance $i_o/v_{gC}$:"

Equation 4.47:

$$A_{OL} = \frac{i_o}{i_c} = -i_{ro1}(-A_V) \left( \frac{i_o}{v_{gC}} \right) = r_{o1} \left[ g_{mA}(r_{dsA} || r_{sd3}) \right] \left( \frac{g_{mC}}{1 + g_{mC}r_{o1}} \right) = g_{mA}(r_{dsA} || r_{sd3})$$

Page 169, 1st paragraph, line 3: “…or $r_{dsCA_V}$, where $A_V$ is $g_{mA}(r_{dsA} || r_{sd3})$:"

Page 185, Active LHP Zeros, line 5: “…equivalent pole-zero pair $p_{z-p} - z-p$ results because…”

Page 186, paragraph 2, line 6: “…(i.e., $1/2\pi R_1 C_1$) until the gain reaches the amplifier’s maximum possible gain $A_{V,OL}$, beyond which point the close-loop gain drops with $A_{V,OL}$, as shown in Fig. 4.25b.”
Figure 5.10:

\[ V_{\text{Bias}} \]

\[ V_{\text{BiasD}} \]

\[ \text{MD1, MD2, MM1, MM2, MTail} \]

Equation 6.8:

\[ \text{LG}_{+FB} \approx G_{+FB}Z_{O.BUF} = \frac{G_{+FB}R_{O.BUF}}{\frac{\text{LG}_{\text{REG}} + 1}{\text{LG}_{\text{REG}} + 1} + \frac{R_{O.BUF}C_{SW}}{\text{LG}_{\text{REG}} + 1}} < 1 \]
Appendix A

Derivation: Time Linear Regulators Require to Respond to a Sudden Load-current Step

A regulator, in essence, is a differential amplifier used in a non-inverting feedback configuration. As such, an equivalent gain block with a reference voltage as its non-inverting input can model its closed-loop response. Figure A.1 illustrates the circuit and its model. The output of the regulator is loaded with a capacitor having a finite ESR value and a current sink characterized by transient load-current steps. Capacitor $C_O$, at first charged to $V_{OUT}$, initially provides the current demanded by the transient load because the regulator requires some time to react. Voltage $v_{OUT}$ therefore instantaneously drops a voltage equal to the product of the load current and the ESR of $C_O$. Consequently, voltage $v_X$ instantaneously drops an attenuated version of the same. This voltage change will be considered, for this derivation, the transient stimulus against which the circuit must react to maintain a regulated output voltage. For analysis, the stimulus is referred back to $V_{REF}$ by simply inverting the polarity of the instantaneous voltage change. This procedure allows the circuit to be modeled, as shown in the figure, by a block having the closed-loop transfer function displayed from $V_{REF}$ to $v_{OUT}$ with a transient voltage step as its stimulus. In this manner, the response time (system delay) to a load-current change may be approximated.
Figure A.1. Block-model development of a typical linear regulator for estimating the time delay through the system.

For simplicity, the circuit is further assumed to exhibit a single-pole response. This assumption is reasonable if any secondary pole is sufficiently displaced from the system’s dominant pole. As a result, the output is expressed as a function of input \( v_{IN} \) and time constant \( \tau \):

\[
v_{OUT} = v_{IN} \left( \frac{A}{1 + A\beta} \right) = \frac{v_{IN}}{\beta} \left( \frac{1}{s\tau + 1} \right), \tag{A.1}
\]

where \( \tau = 1/\omega_{BW} \), \( \omega_{BW} \) the bandwidth in radians, \( A \) the forward open-loop gain of the regulator and \( \beta \) the feedback gain factor or \( R_2 / (R_1 + R_2) \). Figure A.2 shows the time-dependent waveforms of the load current, the consequential input referred voltage, and the output. The input referred signal is further simplified to a single step response \( (v_{IN}') \). This approximation is done since only the delay associated with the instantaneous voltage change is pursued: approximate delay through the system for a single event. The peak-peak voltage of the step response, \( 1 / s \) in the \( s \) domain, is assumed to be 1 V; thus, \( v_{OUT} \) is

\[
v_{OUT} = \frac{1}{s\beta} \left( \frac{1}{s\tau + 1} \right) = 1/\beta \left[ \frac{1}{s} - \left( \frac{\tau}{s\tau + 1} \right) \right] = \frac{1}{\beta} \left[ \frac{1}{s} - \left( \frac{1}{s + 1/\tau} \right) \right], \tag{A.2}
\]

in the \( s \) domain, or equivalently,

\[
v_{OUT} = \frac{1}{\beta} \left[ 1 - \exp \left( -\frac{t}{\tau} \right) \right] \tag{A.3}
\]

in the time domain, where \( t \) refers to time. Consequently, time delay \( t_{delay} \) is the time span defined by the onset of the input transition to the time the output reaches 90% of its final value (i.e., \( 0.9 / \beta \)),

\[
v_{OUT} \left[ \frac{0.9}{\beta} \right] = \frac{1}{\beta} \left[ 1 - \exp \left( -\frac{t_{delay}}{\tau} \right) \right] \tag{A.4}
\]

or

\[
t_{delay} = t_{90\%} = \tau \ln 10 = 2.3\tau = \frac{2.3}{\omega_{BW}}. \tag{A.5}
\]

Consequently, the approximate time delay through the regulator is \( 2.3 / \omega_{BW} \), or equivalently, \( 0.37 / f_{BW} \).
Figure A.2. Time-domain description of the system under a stepped load-current change.