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Rincon-Mora

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(54) **INTEGRATED LOW RIPPLE, HIGH FREQUENCY POWER EFFICIENT HYSTERETIC CONTROLLER FOR DC-DC CONVERTERS**

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This patent is subject to a terminal disclaimer.

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(52) **U.S. Cl.** **323/282**

(58) **Field of Search** 323/280, 282, 323/284, 351

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(57) **ABSTRACT**

The present invention relates to a method of improving power efficiency in a converter circuit at low load currents. The method comprises the steps of monitoring a load current of the converter circuit and adjusting a natural frequency of the converter circuit based on the load current. Such an adjustment of the natural frequency results in a reduction in switching losses at low load currents, thereby improving the power efficiency associated therewith. The present invention also relates to a circuit for improving a power efficiency in a dc—dc converter. The circuit comprises a converter circuit and a comparator circuit coupled to an input of the converter circuit. The dc—dc converter also comprises a feedback circuit coupled between an input and an output of the comparator circuit; the feedback circuit is operable to alter a trip frequency of the comparator circuit as a function of a load current at an output of the converter circuit, thereby decreasing switching losses at low load currents and improving the power efficiency associated therewith.

30 Claims, 6 Drawing Sheets



