The present invention involves a hysteretic comparator (100) for comparing a sample voltage (V_{OUT}) to a reference voltage (V_{REF}). A hysteresis voltage generator providing a voltage V_{Hyst}, and a voltage V_{Hyst+}. A first differential input stage (505) generates a signal coupled to a summing node (506, 507) determined from a difference between the sample voltage and V_{REF}. A second differential input stage (504) generates a signal coupled to the summing node determined from a positive difference between V_{Hyst} and V_{Hyst+}. A third differential input stage (503) generates a signal coupled to the summing node determined from a negative difference between V_{Hyst} and V_{Hyst+}. A control device (512, 513, 514) coupled to selectively enable the second and third differential input stages to select among a first mode and second mode.
FIG. 1

FIG. 2

FIG. 3

FIG. 4
ACCURATE, FAST, AND USER PROGRAMMABLE HYSTERETIC COMPARATOR

This application claims priority under 35 USC § 119(e)(1) of provisional application No. 60/070,035 filed Dec. 30, 1997.

A. BACKGROUND OF THE INVENTION

1. Field of the Invention
The present invention relates, in general, to integrated circuits and, more particularly, to integrated circuits having voltage regulator circuits generating an internal power supply voltage from an external power supply voltage.

2. Relevant Background
Integrated circuits (ICs) comprise thousands or millions of individual devices interconnected to provide desired functionality. Significant effort is expended to improve processing techniques so as to reduce the size of each individual device in order to provide greater functionality on a given IC chip at reduced cost. In general, smaller geometry devices operate faster while dissipating less power than do larger geometry devices. As device geometries are reduced the breakdown voltages of the devices and the isolation that separates the devices decreases also.

Electronic systems usually comprise ICs manufactured with a variety of technologies. This has created a need for multiple power supply voltages to be supplied to a single printed circuit board to support the various types of devices on that board. For example, devices are available that require a power supply voltage ranging from 5.0 volts to 3.3 volts, 2.8 volts or lower. A practical solution to this disparity is to provide voltage regulator circuitry that decreases the higher voltage (e.g., 5.0 V in the above example) to the lower voltage required by small geometry devices (e.g., 3.3 V or 2.8 V). Hence, it is necessary to regulate the available power supply voltage to provide voltages consistent with that required by each of the small geometry ICs.

A conventional voltage regulator is designed to generate a lower voltage than the available supply voltage. Typically, a transistor is coupled in series between the external voltage node and the internal voltage supply node. The conductivity of the transistor is modulated to drop the excess voltage across the transistor. Linear regulators have many desirable characteristics such as simplicity, low output ripple, high quality line and load regulation, and fast recovery time. However, linear regulators are inefficient resulting in wasted power and excess heat generation.

Switching regulators are becoming more common because of their characteristic high efficiency and high power density (i.e., power-to-volume ratio) resulting from smaller magnetic, capacitive, and heat sink components. Switching regulators convert one DC voltage into another DC voltage by selectively storing energy by switching energy on and off in an inductor. By comparing the output voltage to a reference voltage the inductor current is controlled to provide the desired output voltage.

Switching regulators exhibit longer hold-up times than linear regulators which is a characteristic that is important in computer applications. Switching regulators accept a wider range of input voltages with little effect on efficiency making them particularly useful in battery powered applications. However, peak-to-peak output voltage ripple of a switching regulator is typically greater than that of linear regulators. Hence, significant development effort is directed at reducing the voltage ripple of switching regulators.

To limit undesirable voltage ripple on the internal voltage supply node, the time constant of the regulator is desirably much longer than the internal cycle of the loading device. This prevents undesired voltage ripple within a cycle that can upset analog voltage levels. One way of controlling ripple is to heavily filter the regulator output by coupling a large capacitor between the internal voltage supply node and ground. In practice, however, filter capacitors consume a great deal of area without adding functionality. Cost and circuit size considerations dictate limiting the filter capacitor to more modest sizes. Hence, it is desirable to minimize ripple in ways that do not require large filter capacitors.

Another technique to effectively increase the time constant of the regulator is to use hysteretic comparators to compare the output voltage to a reference voltage. The hysteretic comparator output drives a switching transistor that controls current in the inductor. However, it is difficult to generate accurate hysteresis as well as provide the ability to program the hysteresis using off-chip components. One prior solution is to use a Schmitt trigger with an amplifier/shaper comparator having an output and a non-inverting input brought out to pins of the IC. Although this allows the user to program the hysteresis by connecting the external feedback resistor, in many cases, the internal resistor that defines the hysteresis cannot be connected externally because the reference voltage used is not allocated a pin. As a result, the hysteresis is not accurate because the temperature coefficients of the internal and external resistors do not track. Furthermore, the internal and external resistors do not match because they are physically different. Although this limitation can be overcome by bringing the reference voltage out to a pin of the IC, this solution degrades the system’s noise performance as well as raises the cost to manufacture the device. Moreover, the load capacitance created by the pins is significant making the design more complex in addition to degrading the overall performance device.

Another solution is to provide a regulator with fixed hysteresis (i.e., all hysteresis determining components are located on chip). Some control could be provided by using a digitally controlled hysteresis network to select the value of the hysteresis determining components. As the selection set increases the number of pins required increases. A user could then select the hysteresis value from among a finite number of choices dictated by the digital input of the hysteresis network. Although this solution yields high speed and accuracy, this comes at a cost of limited user programmability and increased pin allocation. For example, for a two-bit word, requiring two input pins, only four hysteretic settings can be programmed.

B. SUMMARY OF THE INVENTION
The present invention involves a hysteretic comparator for comparing a sample voltage to a reference voltage $V_{REF}$. A hysteresis voltage generator providing a voltage $V_{INST}$ and a voltage $V_{INST'}$. A first differential input stage generates a signal coupled to a summing node determined from a difference between the sample voltage and $V_{REF}$. A second differential input stage generates a signal coupled to the summing node determined from a positive difference between $V_{INST}$ and $V_{INST'}$. A third differential input stage generates a signal coupled to the summing node determined from a negative difference between $V_{INST}$ and $V_{INST'}$. A control device coupled to selectively enable the second and third differential input stages to select among the first mode and second mode.

In another aspect, the present invention involves a method of generating a pulse width modulated signal for driving an
output stage of a DC regulator. The DC regulator includes an input stage receiving an input voltage \( V_{IN} \) and an output stage providing an output voltage \( V_{OUT} \). A reference voltage \( V_{REF} \) and a hysteresis voltage \( V_{HYS} \) are generated. \( V_{OUT} \) to \( V_{REF} \) are compared to determine a difference signal. In a first mode, \( V_{HYS} \) is added to the difference signal to generate a trigger signal. In a second mode \( V_{HYS} \) is subtracted from the difference signal to generate the trigger signal. The pulse width modulated signal is generated by amplifying the trigger signal.

C. BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a portion of the present invention schematically;

FIG. 2 illustrates an exemplary implementation for generating hysteresis voltages in accordance with the present invention;

FIG. 3 illustrates an other schematic representation of the hysteretic comparator in accordance with the present invention;

FIG. 4 shows a voltage diagram illustrating switching behavior of a hysteretic comparator in accordance with the present invention;

FIG. 5 illustrates an exemplary CMOS implementation in accordance with the present invention;

FIG. 6 illustrates a portion of an alternative embodiment including a BiCMOS implementation in accordance with the present invention;

FIG. 7 shows an example output stage useful in combination with a hysteretic comparator of FIG. 4; and

FIG. 8 shows an alternative output stage useful in combination with a hysteretic comparator of FIG. 4.

D. DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention allows the user to program the hysteresis by connecting two external resistors to two pins of the IC. This feature of the present invention enables a great deal of user flexibility in programming hysteresis to meet the needs of a particular application. The use of two pins does not incur any additional cost compared to prior solutions. Moreover, the time sensitive nodes of the hysteretic comparator are buffered from these external pins. In particular, a pulse width modulated signal generated by the present invention \( V_{DRIVE} \) need not be coupled to an external I/O pin and so that the signal node will not be loaded with capacitance associated with the external I/O pin.

The present invention is illustrated schematically in FIG. 1 as a four-input summing comparator 100. The present invention operates fundamentally as a regulator comprising two distinct regulator elements. A first regulator element is designed to control the average output voltage while a second distinct regulator is designed to control the ripple voltage. The average output voltage is controlled by comparing a reference voltage \( V_{REF} \) to the output voltage \( V_{OUT} \). The ripple regulation is controlled by a \( V_{HYS} \) voltage applied to separate input terminals of comparator 100. In this manner each of the regulator elements in comparator 100 is designed to meet the needs of either an average DC level control or ripple control. Significantly, because the two regulator elements are formed on a single integrated circuit the component devices are closely parametrically matched to provide superior performance.

FIG. 2 illustrates an exemplary circuit used to generate \( V_{HYS} \) from \( V_{REF} \). \( V_{REF} \) is buffered by amplifier 204 so that \( V_{REF} \) is minimally affected by the generation of \( V_{HYS} \). The voltage across \( R_{EXT} \) 202 in FIG. 2 defines:

\[
V_{HYS} = V_{REF} \left( \frac{R_{EXT}}{R_{EXT}} \right)
\]

where \( V_{HYS} \) determines half the amount of hysteresis exhibited by comparator 100. Reference voltage \( V_{REF} \) is generated by a high quality reference such as a bandgap reference. Thus both \( V_{REF} \) and \( V_{HYS} \) will be suitably stable. In a particular implementation shown in FIG. 2, a differential amplifier 204 has a non-inverting input coupled to \( V_{REF} \) and an inverting input coupled to a first I/O node 207. A switch 205 such as an n-channel MOS transistor has a control input coupled to the output of differential amplifier 204. A resistor \( R_{EXT} \) 202 is coupled between the first and second I/O nodes 207 and 206. A resistor \( R_{EXT} \) 201 is coupled between second I/O node 207 and a ground or common potential. A voltage divider formed by the first and second resistor provides the voltage \( V_{HYS} \) on first I/O node 206 and the voltage \( V_{HYS} \) on second I/O node 207.

Switch 205 supplies a controlled current that can be mirrored to supply a stable bias current \( I_{偏} \) described by the formula:

\[
I_{偏} = \left( \frac{V_{REF}}{R_{EXT}} \right) \times K
\]

where \( K \) is a constant determined by the size ratios of the transistors in current mirror 203. This feature of the present invention generates a stable \( I_{偏} \) that can be used by other circuitry and that is also programmable through selection of \( R_{EXT} \) 201 and \( R_{EXT} \) 202. Alternatively node 208 is shorted to the voltage supply \( V_{DD} \). The circuit of FIG. 2 generates a single \( V_{HYS} \) for a symmetric hysteretic comparator 100. The circuit of FIG. 2 can be readily modified to generate distinct \( V_{HYS}^+ \) and \( V_{HYS}^- \) to enable asymmetric operation.

In a preferred implementation, converter 100 is implemented on a monolithic integrated circuit, the first and second I/O nodes 206 and 207 comprise external I/O pins of the integrated circuit. In this embodiment resistors \( R_{EXT} \) and \( R_{EXT} \) are implemented externally with respect to the integrated circuit. A significant advantage in accordance with the present invention is that the hysteresis voltage can be set to any value using two external resistors that can be more closely matched than could an external and internal resistor pair. However, only two I/O pins are required to generate a wide range of hysteresis voltages. Prior art can only provide four hysteretic settings with two input pins. Using the circuit shown in FIG. 2, \( V_{HYS} \) is set independently of the value of \( V_{REF} \) and does not load or alter \( V_{REF} \). Similarly, the capacitance associated with external I/O pins 206 and 207 is buffered from \( V_{REF} \) and so will have minimal impact on performance. As shown in FIG. 1, \( V_{HYS}^+ \) and \( V_{HYS}^- \) are inputs to a set of terminals of comparator 100. In accordance with the present invention, the polarity of \( V_{HYS} \) input terminals is dependent on the comparator output \( V_{DRIVE} \). Referring to FIG. 3, comparator 100 is desirably implemented as a summing comparator comprising three pairs of differential inputs and a binary output. In a first of the differential input pairs the non-inverting (+) input terminal is coupled to \( V_{REF} \) and the inverting (−) input is coupled to the actual regulated DC output \( V_{OUT} \). In a second of the differential inputs, the non-inverting (+) input is coupled to the most positive node of \( V_{HYS} \) designated \( V_{HYS}^+ \), for ease of understanding. In
the second differential pair, the inverting (-) input is coupled to the most negative node \( V_{\text{INP}} \) designated \( V_{\text{INP}} \).

In the third differential input pair, the \( V_{\text{INP}} \) coupleings are reversed such that the non-inverting (+) input is coupled to \( V_{\text{INP}} \), and the inverting (-) node is coupled to \( V_{\text{INP}} \).

In accordance with the present invention, comparator 100 is internally coupled to operate in a selected one of at least two operating modes. In a first mode, output \( V_{\text{DRIVE}} \) is a binary function of the sum of the difference voltages of the first and second pairs of differential inputs. In this first mode, the third pair of differential inputs is essentially disabled. In a second mode, the output \( V_{\text{DRIVE}} \) is a binary function of the sum of the difference voltages of the first and third pairs of differential inputs with the second pair of differential inputs essentially disabled. The operation mode of comparator 100 is selected by the state of \( V_{\text{DRIVE}} \) as coupled back to comparator 100 on feedback line 301.

The voltage at which the binary output of comparator 100 switches is referred to as the "trip-point". The trip-point is centered at \( V_{\text{REF}} \) as shown in FIG. 4. In accordance with the present invention, the trip-point of comparator 100 is offset from \( V_{\text{REF}} \) by an amount \( \Delta V \) equal to \( V_{\text{INP}} \) when \( V_{\text{OUTPUT}} \) is ramping up from a low state and offset from \( V_{\text{REF}} \) by an amount \( \Delta V \) equal to \( V_{\text{INP}} \) when \( V_{\text{OUTPUT}} \) is ramping down from a high state. The trip-point offset \( \Delta V \) is substantially equal (in both directions) to \( V_{\text{INP}} \) when the input pairs in comparator 100 are matched. Alternatively, \( V_{\text{INP}} \) and \( V_{\text{INP}} \) can be set separately for asymmetrical hysteresis operation as described hereinbefore. The benefits of the present invention are greatly exploited in hysteretic DC-DC converters where the accuracy and speed of the comparator are paramount.

FIG. 5 through FIG. 7 show specific CMOS implementations of the present invention. It should be understood that the implementations shown in FIG. 5 through FIG. 7 are provided for example only and that the present invention may be implemented in other technologies including bipolar and BiCMOS technologies, and may use circuits having a greater or lesser number of components to realize the functionality described herein. Indeed, it is possible that the implementations are equivalent to the specific implementations described herein.

Comparator block 501 comprises a CMOS comparator accepting a DC input voltage such as \( V_{\text{INP}} \) that is different from the desired output voltage \( V_{\text{OUT}} \). \( V_{\text{INP}} \) is a typical input voltage and may be higher or lower than \( V_{\text{OUT}} \) although it is higher than \( V_{\text{OUT}} \) in the particular example herein. The trip-point of comparator 501 is set by the signal (i.e., voltage and/or current) on nodes 506 and 507 as set by input differential pairs 503, 504, and 505. Transistors 508, 509, and 511 serve as matched current sources for each of input differential pairs 503, 504 and 505 respectively. Output buffer 502 is implemented as a CMOS buffer having an inverting output stage comprising transistors sized to adequately drive the \( V_{\text{DRIVE}} \) signal.

Output buffer 502 is switched by the output of the comparator block 501. Output buffer 502 generates the \( V_{\text{DRIVE}} \) signal that is coupled back to inverter 512 and mode control switch 514. The output of inverter 512 is coupled to mode control switch 513. Mode control switches 513 and 514 in cooperation with inverter 512 selectively enable one or the other of input pairs 503 and 504 based upon the current binary value of \( V_{\text{DRIVE}} \).

Input pair 505 accepts the \( V_{\text{REF}} \) signal on its non-inverting (+) input and the \( V_{\text{OUT}} \) signal on its inverting input. A first output of input pair 505 is coupled to summing node 506 whereas a second output of input pair 505 is coupled to summing node 507. Input pair 503 accepts the \( V_{\text{INP}} \) signal on its inverting input and the \( V_{\text{INP}} \) signal on its non-inverting input. Input pair 504 accepts the \( V_{\text{INP}} \) signal on its inverting input and the \( V_{\text{INP}} \) signal on its non-inverting input.

In operation, the \( V_{\text{DRIVE}} \) signal selectively enables one or the other of input pairs 503 and 504. In the example shown in FIG. 5, a logic HIGH on the \( V_{\text{DRIVE}} \) line enables switch 514 and disables switch 513. In this first mode, input pair 513 is disabled and does not affect the voltage on summing nodes 506 and 507. In the first mode \( V_{\text{INP}} \) is added to \( V_{\text{REF}} \) to set the trip-point of comparator unit 501. In contrast, a logic LOW on the \( V_{\text{DRIVE}} \) line enables switch 513 and disables switch 514. In this second mode, input pair 514 is disabled and does not affect the voltage on summing nodes 506 and 507. In the second mode \( V_{\text{INP}} \) is subtracted from \( V_{\text{REF}} \) to set the trip-point of comparator unit 501.

FIG. 6 shows a portion of an alternative embodiment illustrating two alternative features in accordance with the present invention. The circuit of FIG. 6 illustrates a bipolar-CMOS (BiCMOS) implementation including both bipolar and CMOS components. The circuit shown in FIG. 6 performs essentially the same functions as the circuit shown in FIG. 5. However, input differential amplifiers 603 and 605 are implemented using bipolar NPN transistors which offer faster switching characteristics than the MOS implementation of FIG. 5. Details of biasing differential pairs 603 and 605 are not significant for the understanding of the present invention and so are not shown in this illustrative embodiment. Any available biasing technique may be used to supply \( I_{\text{BIAS1}} \) and \( I_{\text{BIAS2}} \).
a switch 701 implemented as an n-channel MOSFET. The buck regulator of FIG. 7 is used to step an input voltage \( V_{IN} \) down to a lower level. Switch 701 chops the input DC voltage \( V_{IN} \) into a square wave. This square wave is then converted back into a DC voltage of lower magnitude by the low pass filter comprising inductor 702 and capacitor 703. Diode 704 shunts excess voltage to ground while capacitor 706 serves as a preliminary filter to smooth variations in \( V_{IN} \). The duty cycle of the square wave relates the output voltage to the input voltage by the equation:

\[
V_{OUT} = V_{IN} \times \frac{t_{on}}{t_{on} + t_{off}}
\]

where \( t_{on} \) and \( t_{off} \) describe the duty cycle of \( V_{DRIVE} \).

FIG. 8 shows a synchronous buck power stage used to efficiently convert the input voltage \( V_{IN} \) down to a lower DC voltage \( V_{OUT} \). In this implementation transistors 801 and 702 receive independent drive signals from dead time control circuit 806 based upon \( V_{DRIVE} \). Switches 801 and 802 chop the input DC voltage \( V_{IN} \) into a square wave. This square wave is then converted into a DC voltage of lower magnitude by a low pass filter comprising inductor 803 and capacitor 804.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

What is claimed is:

1. A hysteretic comparator for comparing a sample voltage comprising:
   a reference voltage generator providing a voltage \( V_{REF} \);
   a hysteresis voltage generator providing a voltage \( V_{HYS} \);
   a first differential input stage generating a signal coupled to a summing node determined from a difference between the sample voltage and \( V_{REF} \);
   a second differential input stage generating a signal coupled to the summing node determined from a positive difference between \( V_{HYS} \) and \( V_{REF} \);
   a third differential input stage generating a signal coupled to the summing node determined from a negative difference between \( V_{HYS} \) and \( V_{REF} \);
   a control device coupled to selectively enable the second and third differential input stages to select among a first mode and a second mode wherein the hysteresis voltage generator derives \( V_{HYS} \) and the voltage \( V_{HYS} \) from \( V_{REF} \).

2. A hysteretic comparator for comparing a sample voltage comprising:
   a reference voltage generator providing a voltage \( V_{REF} \);
   a hysteresis voltage generator providing a voltage \( V_{HYS} \);
   a first differential input stage generating a signal coupled to a summing node determined from a difference between the sample voltage and \( V_{REF} \);
   a second differential input stage generating a signal coupled to the summing node determined from a positive difference between \( V_{HYS} \) and \( V_{REF} \);
   a third differential input stage generating a signal coupled to the summing node determined from a negative difference between \( V_{HYS} \) and \( V_{REF} \);
   a control device coupled to selectively enable the second and third differential input stages to select among a first mode and a second mode wherein the hysteresis voltage generator derives \( V_{HYS} \) and the voltage \( V_{HYS} \) from \( V_{REF} \).

3. The hysteretic comparator of claim 2 wherein the hysteretic voltage generator is implemented on a monolithic integrated circuit, the first and second I/O nodes comprise external I/O pins of the integrated circuit, and the first and second resistors are implemented externally with respect to the integrated circuit.

4. A hysteretic comparator for comparing a sample voltage comprising:
   a reference voltage generator providing a voltage \( V_{REF} \);
   a hysteresis voltage generator providing a voltage \( V_{HYS} \) and a voltage \( V_{HYS} \);
   a first differential input stage generating a signal coupled to a summing node determined from a difference between the sample voltage and \( V_{REF} \);
   a second differential input stage generating a signal coupled to the summing node determined from a positive difference between \( V_{HYS} \) and \( V_{REF} \);
   a third differential input stage generating a signal coupled to the summing node determined from a negative difference between \( V_{HYS} \) and \( V_{REF} \);
   a control device coupled to selectively enable the second and third differential input stages to select among a first mode and a second mode wherein the control device further comprises:
   an inverter coupled to receive a \( V_{DRIVE} \) signal and generate an inverted \( V_{DRIVE} \) signal;
   a first switch coupled to controllably interrupt current in the second input stage, the first switch under control of the \( V_{DRIVE} \) signal; and
   a second switch coupled to controllably interrupt current in the third input stage, the second switch under control of the inverted \( V_{DRIVE} \) signal.

5. The hysteretic comparator of claim 4 wherein the first, second, and third input stages each have a non-inverting output and an inverting output, and the hysteretic comparator further comprises:
   a first summing node coupled to the non-inverting output of the first input stage, the non-inverting output of the second input stage, and the inverting output of the third input stage; and
   a second summing node coupled to the inverting output of the first input stage, the inverting output of the second input stage, and the non-inverting output of the third input stage.

6. A method of generating a pulse width modulated signal for driving an output stage of a regulator, the regulator including an input stage receiving an input voltage \( V_{IN} \) and an output stage providing an output voltage \( V_{OUT} \), the method comprising the steps of:
generating a reference voltage $V_{\text{REF}}$;
generating a hysteresis voltage $V_{\text{HYST}}$;
comparing $V_{\text{OUT}}$ to $V_{\text{REF}}$ to determine a difference signal;
in a first mode, adding $V_{\text{HINST}}$ to the difference signal to
generate a trigger signal;
in a second mode, subtracting $V_{\text{HINST}}$ from the difference
signal to generate the trigger signal; and
generating the pulse width modulated signal by amplifying
the trigger signal further comprising the steps of:
chopping the input voltage $V_{\text{IN}}$ into a square wave
using the pulse width modulated signal; and
converting the square wave into the voltage $V_{\text{OUT}}$ using
a low pass filter.

7. A DC-DC converter comprising:
an input node receiving an input voltage $V_{\text{IN}}$;
a pulse width modulation (PWM) unit coupled to chop
$V_{\text{IN}}$ into a square wave under control of a $V_{\text{DRIVE}}$
signal;
an output stage converting the chopped $V_{\text{IN}}$ to an output
voltage $V_{\text{OUT}}$ (coupled to an output node);
a reference voltage generator providing a voltage $V_{\text{REF}}$;
a hysteresis voltage generator providing a voltage $V_{\text{HINST}}$;
and a voltage $V_{\text{HINST}}$; and
a hysteresis comparator unit coupled to receive $V_{\text{OUT}}$,
$V_{\text{REF}}$, $V_{\text{HINST}}$, and $V_{\text{HINST}}$ and coupled to the PWM
unit to provide the $V_{\text{DRIVE}}$ signal, the hysteresis com-
parator having a first mode and a second mode selected
by the $V_{\text{DRIVE}}$ signal.

8. The DC-DC converter of claim 7 wherein the hysteretic
comparator further comprises:
a first differential input stage generating a signal coupled
to a summing node determined from a difference
between $V_{\text{OUT}}$ and $V_{\text{REF}}$;
a second differential input stage generating a signal
coupled to the summing node determined from a pos-
tive difference between $V_{\text{HINST}}$ and $V_{\text{HINST}}$;
a third differential input stage generating a signal coupled
to the summing node determined from a negative
difference between $V_{\text{HINST}}$ and $V_{\text{HINST}}$; and
a control device coupled to selectively enable the second
and third differential input stages to select among the
first mode and second mode.

9. The DC-DC converter of claim 2 wherein the first
two and third input stages each have a non-inverting
output and an inverting output, and the summing node
further comprises:
a first summing node coupled to the non-inverting output
of the first input stage, the non-inverting output of the
second input stage, and the inverting output of the third
input stage; and
a second summing node coupled to the inverting output of
the first input stage, the inverting output of the second
input stage, and the non-inverting output of the third
input stage.

10. The DC-DC converter of claim 8 wherein the control
device further comprises:
an inverter coupled to receive the $V_{\text{DRIVE}}$ signal and
generate an inverted $V_{\text{DRIVE}}$ signal;
a first switch coupled to controllably interrupt current in
the second input stage, the first switch under control of the
$V_{\text{DRIVE}}$ signal; and
a second switch coupled to controllably interrupt current
in the third input stage, the second switch under control of
the inverted $V_{\text{DRIVE}}$ signal.

11. The DC-DC converter of claim 8 further comprising:
first, second, and third matched current sources regulating
current in each of the first, second, and third input
stages respectively.

12. The DC-DC converter of claim 9 wherein the hyste-
retic comparator further comprises:
a fourth differential comparator generating a binary signal
from a difference between the first and second sum-
mung nodes; and
an output driver coupled to receive the binary signal from
the fourth differential comparator and generate the
$V_{\text{DRIVE}}$ signal.

13. The DC-DC converter of claim 7 wherein the hysteretic
comparator further comprises:
a first differential input stage generating a signal coupled
to a summing node determined from a difference
between $V_{\text{OUT}}$ and $V_{\text{REF}}$;
a second differential input stage generating a signal deter-
mimed from a difference between $V_{\text{HINST}}$ and $V_{\text{HINST}}$;
a current steering unit coupled to add the signal from the
second differential input stage to the summing node in
the first mode and subtract the signal from the second
differential input stage from the summing node in the
second mode; and
a control device coupled to the current steering unit to
select among the first mode and second mode.

14. The DC-DC converter of claim 9 wherein the hysteretic
voltage generator further comprises:
a differential amplifier having a non-inverting input
coupled to $V_{\text{REF}}$ and an inverting input coupled to a
first I/O node, and an output;
a switch having a control input coupled to the differential
amplifier output, the switch supplying a controlled
current to a second I/O node;
a first resistor coupled between the first and second I/O
nodes;
a second resistor coupled between the second I/O node
and a ground potential; and
wherein a voltage divider formed by the first and second
resister provide the voltage $V_{\text{HINST}}$ on the first I/O node
and the voltage $V_{\text{HINST}}$ on the second I/O node.

15. The DC-DC converter of claim 14 wherein the converter
is implemented on a monolithic integrated circuit, the
first and second I/O nodes comprise external I/O pins of
the integrated circuit, and the first and second resistors are
implemented externally with respect to the integrated
circuit.
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page.
Item [75], change Ricon-Mora to -- Rincon-Mora --

Signed and Sealed this
Twenty-ninth Day of January, 2002

Attest:

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

Attesting Officer