LOW DROP-OUT VOLTAGE REGULATOR
WITH PMOS PASS ELEMENT

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ABSTRACT
A voltage regulator circuit includes: a first MOS transistor 12 coupled between a voltage supply line and an output node 44, the first MOS transistor 12 providing a stable voltage on the output node 44; a source follower 24 coupled to a gate of the first MOS transistor 12; an amplifier 38 coupled to a gate of the source follower 24 for controlling the response of the first MOS transistor 12; negative feedback circuitry coupled between the output node 44 and the amplifier 38, the feedback circuitry providing feedback to the amplifier 38; a current conveyor 46 coupled to the first MOS transistor 12; and positive feedback circuitry 26 coupled between the current conveyor 46 and the source follower 24.

5 Claims, 1 Drawing Sheet