GEORGIA INSTITUTE OF TECHNOLOGY
School of Electrical and Computer Engineering

ECE 6412 **ANALOG INTEGRATED-CIRCUIT DESIGN** **Summer 2025**

INSTRUCTOR: Prof. Gabriel A. Rincón-Mora, Ph.D.
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URL: Rincon-Mora.gatech.edu

LECTURES: Mondays/Wednesdays at 3:30–5:40 p.m. in Van Leer C456

OFFICE HOURS: Course Questions: Q & A Sessions on Tuesdays at 7:30 p.m. with Zoom
Academic Standing/Personal Matters: Send e-mail for consultation

COURSE URL: Rincon-Mora.gatech.edu/classes

SYLLABUS: Linked under "ECE 6412 Analog Integrated Circuit Design" link

COURSE DESCRIPTION: ECE 6412 extends the concepts of semiconductor devices, integrated circuits (ICs), and applications begun in ECE 3040, ECE 3400, and ECE 4430. The material presents, explains, and shows how to understand, develop, and use semiconductor devices to model, analyze, and design transistor-level analog ICs with and without feedback using bipolar and CMOS technologies. The underlying aim is to cultivate and develop insight and intuition for how semiconductor devices work individually and collectively in microelectronic circuits. The material presents an engineering perspective on design that transcends math and fosters innovation.

PREREQUISITE: ECE 4430 Analog Integrated Circuits or equivalent

EDUCATIONAL OUTCOMES: Upon successful completion of this course, students should be able to:
1. Analyze and design operational amplifiers.
2. Analyze and design linear voltage regulators.
3. Analyze and design comparators.
4. Analyze and design reference circuits.

GRADE COMPOSITION:

Midterm Exam	= 30%
Final Exam	= 35%
Assignments	= 30%
Class Attendance/Professionalism (Adherence to syllabus & ECE policies)	= 5%

Possible extra credit for distinguishably extraordinary effort.

IMPORTANT DATES:

First Day of Class	May 12 (Monday)
Midterm Exam	June 23 (Monday)
Last Day to Drop Course	June 28 (Saturday)
School Recess	May 26 (Monday)
Last Day of Class	July 21 (Monday) – Last assignment due on this date
Final Exam	TBD

LECTURES FROM: *Analog IC Design*, *Ed. 8, Ver. 2*. NY: KDP (www.amazon.com/dp/B0C6BLTBBL).

REFERENCES: *Switched Inductor Power IC Design*. Springer, 2022 (on-line access with GT Library).
Analog IC Design with Low-Dropout Regulators, *2nd Edition*. McGraw-Hill, 2014.
CMOS Analog Circuit Design, *3rd Edition*. Oxford University Press.
YouTube videos linked on class URL under "…YouTube Videos…" link.

ADVICE: Review material presented after each lecture, write notes, & ask questions.
Bring book to class & annotate on it or refer to it in your notes.

COURSE EXPECTATIONS AND GUIDELINES

*Format

IN CLASS: No recordings/photos allowed.
No auditors allowed.
Be seated & ready before class begins (penalty points for being absent or late).
Cellular phones, laptops, & tablets must be off & out of sight.
No smoking or eating in class.
Students are responsible for all material & information announced in class & with Canvas.

EXAMS: No textbooks or notes allowed.
Calculators cannot be used in programmable mode.
No make-up exams (without prior approval two or more weeks in advance).
In case of medical emergencies, work with the Office of the Dean of Students.
Grades become final one week after exams are graded and returned.
*List problems in numerical order, circle & mark answers clearly, & staple pages together.

ASSIGNMENTS:
No collaboration allowed (unless otherwise stipulated).
No late submissions without prior approval (submit request no later than 48 hours before due date/time).
Allowed late submissions lose 20% for each day they are late (including weekends).
Grades become final one week after they are available.
*Include a cover sheet with the course name and number, your name, date, & assignment number.
*List problems in numerical order & circle & mark answers clearly.

PREPARING FOR CLASS: Review previous lecture & read ahead material to be covered in class.

PREPARING FOR EXAMS: Review lectured slides & notes & re-do examples & assignments with & without the key.

ASSISTANCE: Provided in direct proportion to demonstrated effort
in your own attempts to understand & resolve misunderstandings.

ACADEMIC INTEGRITY: All Georgia Tech (GT) students must know and follow GT's Academic Honor Code (https://catalog.gatech.edu/policies/honor-code). In accordance with the Honor Code, I expect your cooperation in reporting suspicious acts relating to academic misconduct. I must and will therefore report all instances of academic dishonesty to the Office of Student Integrity, who will investigate incidents and mandate appropriate penalties for violations. So out of respect for your peers, professors, Georgia Tech, and alumni, please do not engage in dishonest activities in or outside of class.

STUDENT–FACULTY EXPECTATIONS: At Georgia Tech, we strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and students. See https://catalog.gatech.edu/rules for basic expectations that you can have of me and I of you. Respect for knowledge, hard work, and cordial interactions will help build the environment we seek, so please remain committed to these ideals in and outside of class.

INSTITUTE ABSENCE POLICY: See Georgia Tech's policies on absences at https://catalog.gatech.edu/rules/4.

ACCOMMODATIONS FOR STUDENTS WITH DISABILITIES: If you have learning needs that require special accommodations, schedule an appointment with the Office of Disability Services at disabilityservices.gatech.edu to discuss your needs and send me a note that explains your situation and their recommendations **before the second week of classes begins**.

COURSE OUTLINE

1. Analog Electronics
2. Analog Primitives
3. Feedback
4. Differential Stage
5. Operational Amplifiers
6. Linear Voltage Regulators
7. Comparators
8. Reference Circuits

READING & VIEWING MATERIAL

I. *Switched Inductor Power IC Design*, Springer, 2022 (on-line access with GT Library).
II. *Analog IC Design with Low-Dropout Regulators*, 2th Edition, McGraw-Hill, 2014.
III. *CMOS Analog Circuit Design*, 3rd Edition, Oxford University Press.
IV. YouTube videos linked on class URL under "…YouTube Videos…" link.

Chapter 1. Analog Electronics	
1.1. Electronic Devices	I. Sections 1.2, 1.4, 2.2–2.4; IV. Devices: D3, D5–6, D10, D12
1.2. Transistor Circuits	II. Sections 4.3–4.7; IV. Primitives: X1–5
1.3. Two-Port Models	I. Section 5.1; IV. Frequency: FR1
1.4. Frequency Response	I. Sections 5.2–5.3; II. Section 4.2; IV. Frequency: FR6–7
Chapter 2. Analog Primitives	
2.1. Cascode	III. Section 5.3
2.2. Current Mirror	II. Section 5.1; III. Section 4.4
2.3. E/S-Coupled Pair	II. Section 5.2
2.4. B/G-Coupled Pair	II. Section 5.3
2.5. Simulations	
Chapter 3. Feedback	
3.1. Feedback Loop	I. Section 6.1; II. Section 6.1
3.2. Impedances	II. Section 6.2.2
3.3. Analysis	II. Section 6.4
3.4. Configurations	II. Section 6.3–6.4
3.5. Stability	I. Sub-section 6.1.4, II. Section 6.5; III. Section 6.2
Chapter 4. Differential Stage	II. Sub-sections 5.4.1–5.4.5; III. Section 5.2
4.7. Simulations	III. Section 6.6
Chapter 5. Operational Amplifiers	
5.1. Introduction	III. Section 6.1
5.2. Input	II. Section 5.4.6
5.3. Output	III. Section 5.5
5.4. Class-A Op-Amp Example	III. Section 6.3–6.5
5.5. Class-AB Op-Amp Examples	III. Section 7.1
5.6. Current-Mode Op Amp	III. Section 5.4
Chapter 6. Linear Voltage Regulators	
6.1. Introduction	II. Sections 2.1–2.2, 2.5
6.2. Frequency Response	II. Sections 8.2–8.3
6.3. Power-Supply Rejection	II. Section 8.4
6.4. Design	II. Sections 9.2–9.4
Chapter 7. Comparators	
7.1. Introduction	III. Section 8.1
7.2. Open Loop	III. Section 8.2–8.3
7.3. Hysteretic	III. Section 8.4
7.4. Regenerative	III. Section 8.5
7.5. High Speed	III. Section 8.6
Chapter 8. Reference Circuits	
8.1. Voltage Primitives	II. Section 7.1
8.2. PTAT Core	II. Section 7.2
8.3. Temperature Independence	II. Sections 7.3–7.4
8.4. Current References	II. Section 7.8
8.5. Voltage References	II. Section 7.9