NAME: _____

GEORGIA INSTITUTE OF TECHNOLOGY
School of Electrical and Computer Engineering

ECE 4430 Third Exam Closed Book and Notes
Fall 2002 November 27, 2002

General Instructions:

1. Write on one side of the paper. (1 Pt.)

2. Put answers to all questions in the spaces provided on the test. (1 Pt.)

3. Show all work for full credit on questions requiring calculations. No credit will be given for answers alone, without supporting work.

4. Problems and questions are weighted as indicated. The maximum score is 100 points.

5. If you need more paper (provided in class), remove the staple from the exam and, when finished, arrange the test in order. Place the extra pages with supporting work in the test behind the page where the problem appears and indicate accordingly. Staple the entire test together so that there are no loose pages. (1 Pt.)

TEST SCORE: _____ / 100

I certify that I have neither given nor received any assistance while taking this test from anyone.

_____ (Signature) (1 Pt.)

☐ Place a check mark in the box if you observed any suspicious actions while taking this test.

Formula Sheet: Equations/Constants that you may, or may not, need are listed below:

$K' = 50\ \mu A/V^2$ (unless otherwise stated in the problem)
$K_n = K'W/L$
$\lambda = 0.01\ V^{-1}$ (unless otherwise stated in the problem)
$V_{TO} = 0.7$ V (unless otherwise stated in the problem)
$\gamma = 0.5\ V^{1/2}$ (unless otherwise stated in the problem)
$2\varphi_F = 0.6$ V (unless otherwise stated in the problem)
$I_{D\text{-}Triode} = (K_n/2)\ [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$
$I_{D\text{-}Sat} = (K_n/2)\ (V_{GS} - V_{TN})^2\ (1 + \lambda V_{DS})$
$V_{TN} = V_{TO} + \gamma\ [\text{sqrt}(2\varphi_F - V_{BS}) - \text{sqrt}(2\varphi_F)]$
$r_{o\text{-}MOS} \approx 1 / (\lambda I_{DS})$
$g_{m\text{-}MOS} = \text{sqrt}[2I_{DS}K_n]$
$V_{ds\text{-}sat} = \text{sqrt}(2I_{DS}/K_n)$
$g_{mb\text{-}MOS} = \eta g_{m\text{-}MOS}$
$\eta = \gamma \div 2\ \text{sqrt}(2\varphi_F - V_{BS})$

$V_t = kT/q \approx 26$ mV and $I_S = 1E\text{-}15$ A (unless otherwise stated in the problem)
$I_{Diode} = I_S\ [\exp(V_D/V_t) - 1]$

$$C_j = \frac{C_{j0}}{\left(1 - \frac{v_D}{\psi_o}\right)^m} \qquad \rightarrow 0.33 \le m \le 0.5$$

$V_A = 100$ V (unless otherwise stated in the problem)
$\beta_F = 50$ (unless otherwise stated in the problem)
$I_{CE} = I_S\ [\exp(V_{BE}/V_t) - 1]\ [1 + V_{CE}/V_A]$
$r_{o\text{-}NPN} = V_A / I_{CE}$
$g_{m\text{-}NPN} = I_{CE}/V_t$

$CMRR = |A_{dm}| / |A_{cm}|$

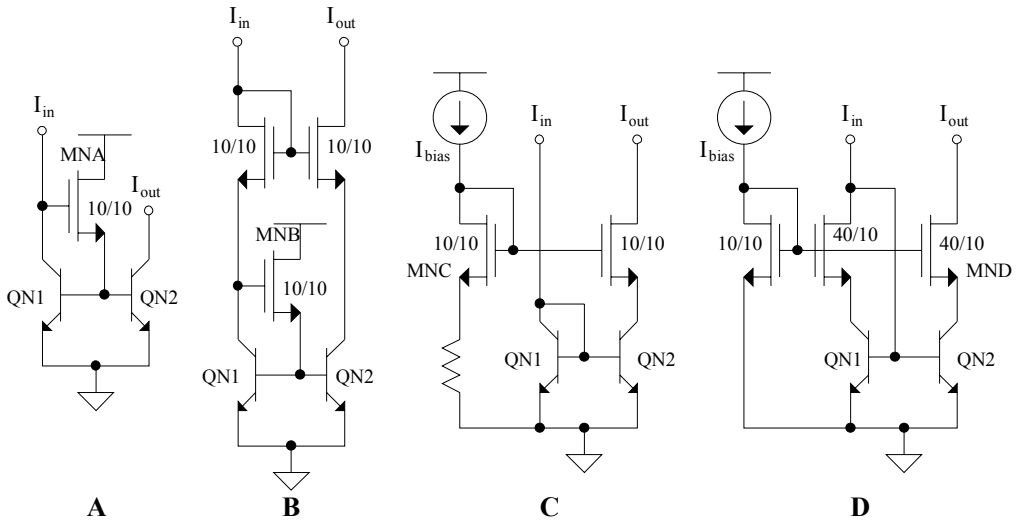
$Z_{miller\text{-}in} = Z / (1 - k)$
$Z_{miller\text{-}out} = Z\ k / (k - 1)$

Current Source/Sink Mirrors – Part A (34 Points)

1. An ideal current mirror has ***high / low*** output resistance. (2 pts)

2. An ideal current mirror has ***high / low*** input resistance. (2 pts)

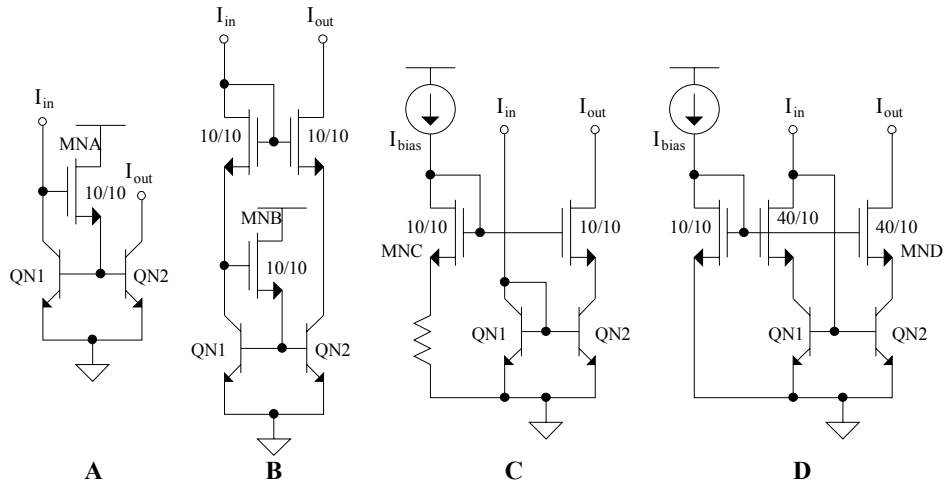
3. Using the figure shown below and assuming that the collector-emitter resistance (r_o) of bipolar transistors is equivalent to the largest possible drain-source resistance (r_{ds}) of MOS devices ($r_{o\_ce} \approx r_{ds\_max} \rightarrow V_A \approx 1/\lambda_{min}$) and the overdrive ($V_{DS\_sat}$) of all MOSFETs is roughly 0.3V, answer the following questions.



a) Why was MNA added to Circuit A? (4 pts)

b) What is the purpose of MNC and the resistor in Circuit C? (4 pts)

c) What is the purpose of MND in Circuit D? (4 pts)



d) Which circuit has the lowest output V_{min} (lowest output voltage possible for which the circuit still operates properly)? (4 pts)

e) Which circuit mirrors the current most accurately ($I_{in} = I_{out}$ –no systematic errors–) and why?

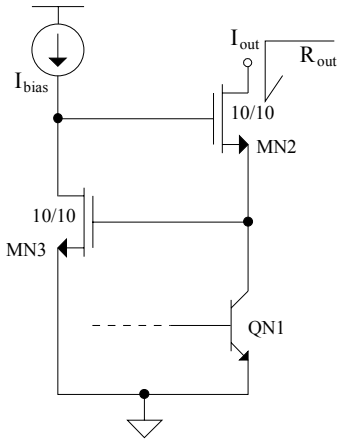
(4 pts)

f) Which circuit has the worst accuracy (with respect to systematic errors only) and why?

(4 pts)

4. Derive the output resistance (R_{out}) of the circuit illustrated below as a function of small-signal parameters r_{o1}, $r_{\pi 1}$, g_{m1}, r_{ds2}, g_{m2}, r_{ds3}, g_{m3}, r_{ds4}, g_{m4}, etc., and assume β is infinite for the NPN transistor.

(6 pts)



Differential Amplifiers – Part B (48 Points)

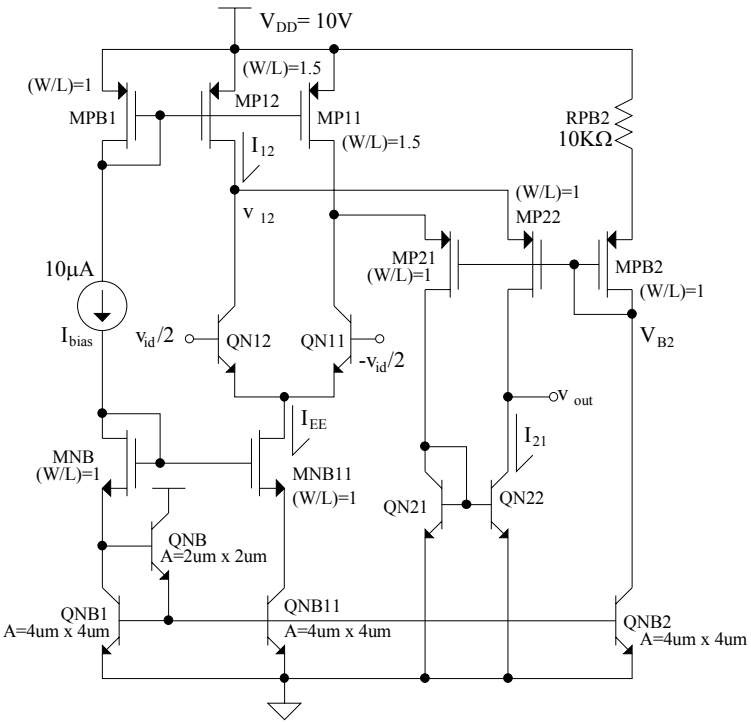
Using the folded-cascode amplifier circuit shown, answer the following questions.

1. What is the purpose of QNB? (4 pts)

2. What is the purpose of MNB11? (4 pts)

3. What is the value of DC current I_{EE}? (4 pts)

(assume β_{NPN} is very large)



4. What is the value of DC current I_{12}? (4 pts)

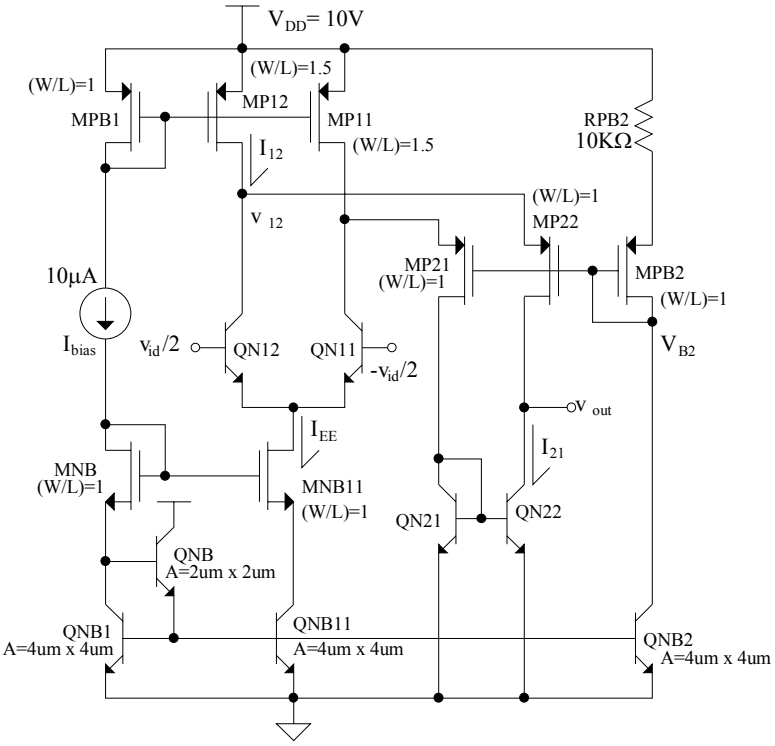
(assume β_{NPN} is very large)

5. What is the value of DC current I_{21}? (4 pts)

(assume β_{NPN} is very large)

6. What is the value of DC voltage V_{B2} (V_{TP} = 1 and k'_P = 20 μA/V^2)? (4 pts)

7. What is the input common-mode voltage range (ICMR) of this circuit, as a function of constants and V_{BE}, V_T, V_{DS_sat}, and V_{CE_min}?

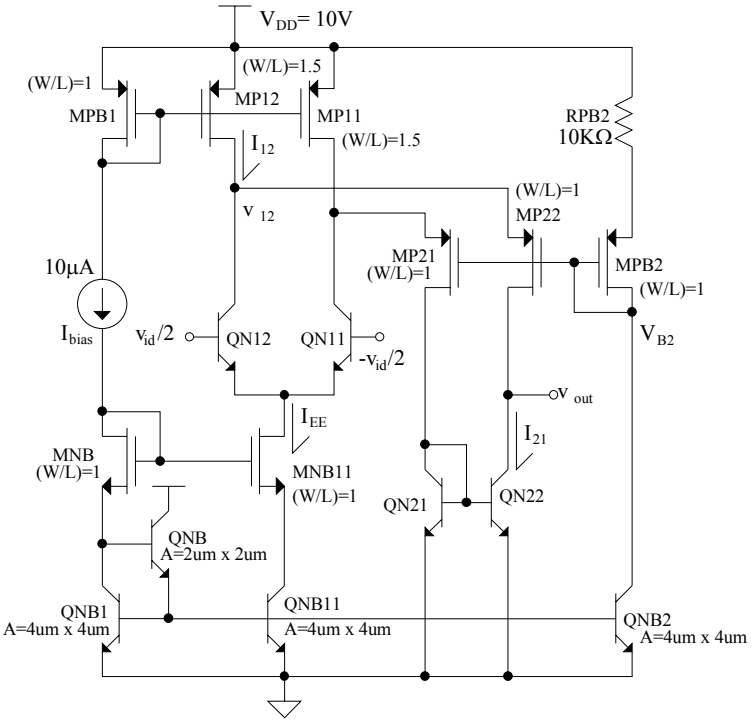


_____ ≤ V_{icm} ≤ _____ (6 pts)

8. What is the maximum output voltage swing of this circuit (output common-mode range OCMR) , as a function of constants and V_T, V_{DS_sat}, and V_{CE_min}?

_____ ≤ V_o ≤ _____ (6 pts)

9. Derive the differential gain to v_{12} (i.e., v_{12}/v_{id}), as a function of g_m, r_{ds}, r_o, r_π, etc.? (6 pts)



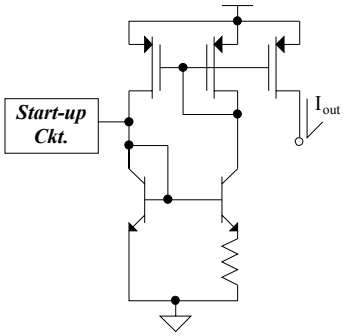
10. Derive the gain from v_{12} to output v_{out} (i.e., v_{out}/v_{12}), as a function of g_m, r_{ds}, r_o, r_π, etc.? (6 pts)

References – Part C (14 Points)

1. An ideal voltage reference has ***high / low*** output resistance. (2 pts)

2. Ideally, the resistance between a voltage reference and the supply voltage is ***high / low***. (2 pts)

3. Why does a bootstrapped reference require a start-up circuit? (4 pts)



4. Given base-emitter ($V_{BE} \rightarrow V_{ref} = AV_{BE}$ or $I_{ref} = V_{BE}/R$) and gate-source ($V_{GS} \rightarrow V_{ref} = AV_{GS}$ or $I_{ref} = V_{GS}/R$) voltage derived reference circuits, the ***base-emitter / gate-source*** derived reference circuits have lower sensitivity to the supply voltage. Explain your answer below. (6 pts)

Part A.

1. High

2. Low

3.a. To eliminate base-current errors

3.b. To bias QN2 with a low V_{CE} → To decrease the output V_{min} of the circuit

3.c. To increase the output resistance of the current mirror circuit

3.d. A

3.e. B → There are no Early voltage errors ($V_{CE1} = V_{CE2}$) and no base-current errors ($I_{CN1} = I_{in}$)

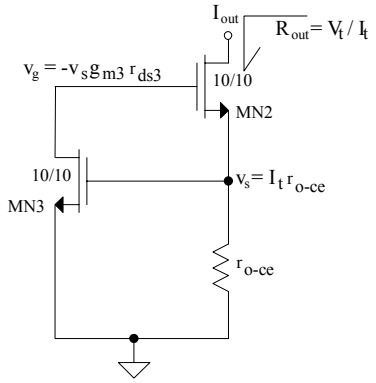
3.f. C → Base-current errors exist as well as Early voltage effects ($V_{CE1} \neq V_{CE2}$)

4. $R_{out} = (I_t - g_{m2}v_{gs2})r_{ds2} / I_t = (I_t - g_{m2}[v_g - v_s])r_{ds2} / I_t$

$$v_g - v_s = -v_s (g_{m3}r_{ds3} + 1) = -I_t r_{o\_ce} (g_{m3}r_{ds3} + 1)$$

→ $$R_{out} = (I_t + g_{m2}[I_t r_{o\_ce} (g_{m3}r_{ds3} + 1)])r_{ds2} / I_t$$

$$= [1 + g_{m2}r_{o\_ce} (g_{m3}r_{ds3} + 1)]r_{ds2}$$



Part B.

1. To reduce base-current errors in the QNB1, QNB11, QNB2 current mirror

2. To increase the output resistance of current sink MNB11, QNB11

3. $I_{EE} = I_{C\_QNB11} = I_{C\_QNB1} \approx 10\ \mu A$ (QNB1,QNB11 is a 1-to-1 current mirror)

4. $I_{12} = 1.5\ I_{D\_MPB1} = 15\ \mu A$ (MPB1, MP12 is a 1-to-1.5 current mirror)

5. $I_{21} = I_{12} - I_{EE}/2 = 10\ \mu A$

6. $V_{B2} = V_{DD} - I_{C\_QNB2} R_{PB2} - V_{SG\_MPB2} = 10 - (10\mu)(10k) - V_{TP} - V_{ON\_MPB2}$

$$= 10 - 0.1 - 1 - \sqrt{\frac{2I}{K_P'(W/L)}} = 8.9 - 1 = 7.9\ V$$

7. $V_{CE\_QNB11} + V_{DS\_MNB11} + V_{BE\_QN12} \leq V_{icm} \leq V_{DD} - V_{SD\_MP12} - V_{CE\_QN12} + V_{BE\_QN12}$

where $V_{CE\_QNB11} = V_{BE\_QNB1} + V_{BE\_QNB}$

$$V_{DS\_sat} + 3V_{BE} \leq V_{icm} \leq 10 - V_{SD\_sat} - V_{CE\_min} + V_{BE}$$

8. $V_{CE\_QN22} \leq V_O \leq V_{DD} - V_{SD\_MP12} - V_{SD\_MP22}$ where $V_{SD\_MP22} \approx I_{C\_QNB2} R_{PB2}$

$$V_{CE\_min} \leq V_O \leq 10 - I_{C\_QNB2} R_{PB2} - V_{SD\_min} = 10 - 0.1 - V_{SD\_min} = 8.9 - V_{SD\_min}$$

9. Since the emitters of QN11 and QN12 are ac-ground with a differential input signal

→ common-emitter gain configuration

$$v_{12} = (v_{id}/2)(-g_{m\_QN12})(r_{o\_QN12}//r_{sd\_MP12}//[1/g_{m\_MP22}]) \approx (v_{id}/2)(-g_{m\_QN12})(1/g_{m\_MP22})$$

$$v_{12}/v_{id} = -g_{m\_QN12}/(2g_{m\_MP22})$$

10. Common-gate gain configuration → $v_{out} \approx v_{12}\, g_{m\_MP22}\, r_{o\_QN22}$ or $v_{out}/v_{12} \approx g_{m\_MP22}\, r_{o\_QN22}$

(the resistance seen into the drain of MP22 is assumed to be much larger than r_{o_QN22} –cascoded resistance → source-degenerated circuit–)

Part C.

1. Low

2. High

3. Bootstrapped references have two or more possible states of operation (e.g., on and off states). Consequently, a start-up circuit is necessary to ensure the circuit operates in the desired state.

4. Base-emitter → An exponentially larger change in current is required to alter V_{BE} whereas MOSFETs require a square-law change to alter V_{GS} → lower output resistance.