CHAPTER 2 – REVIEW PROBLEMS
(READING: Text-Chapter 2)

Chapter 2 Topics

• Integrated Circuit Technology
• Bipolar Technology
• Passive Components in Bipolar Technology
• CMOS Technology
• CMOS Technology-Compatible Devices
• BiCMOS Technology
Problem 1

(a.) Sketch the approximate side view of a NMOS transistor in a p-substrate. Identify each region and identify the connections at the top surface of the integrated circuit for the source, drain, gate and bulk/substrate.

Solution

![NMOS Transistor Diagram](image-url)
Problem 1 - Continued

(b.) Sketch the approximate side view of a NPN vertical transistor in an n-epitaxial region which is on top of a p-substrate. Identify each region (including the n+ buried layer) and identify the connection at the top surface of the integrated circuit for the base, emitter, collector and substrate.

Solution
Problem 2

A layout of a NMOS transistor is shown.

- Find the values of $RD$, and $RS$ in the schematic shown if the sheet resistance of the n$^+$ is 35/µm$^2$ and the resistance of a single contact is 1.

- Find the values of $CBD$ and $CBS$ assuming the transistor is cutoff and the drain and source are at ground potential, if $CJ$ and $CJSW$ for an NMOS transistor are $770 \times 10^{-6}$ F/m$^2$ and $380 \times 10^{-12}$ F/m. Assume the capacitors are lumped and appear on the source/drain side of the bulk resistors in part (a).

- What is the W and L of this transistor?

- If the overlap capacitor/unit length is $220 \times 10^{-12}$ F/m, what is $CGD$?

Fig. F00E2P1

Each square is $1 \mu m \times 1 \mu m$
Problem 2 – Continued

Solution

(a.) The area between the edge of the contacts to the polysilicon is 5µm by 22µm. This represents a bulk resistance of \((5/22) \times 35 \ \mu\text{m}^2 = 7.95 \ \mu\Omega\). Adding 5 contacts in parallel gives

\[
R_D = R_S = 7.95 + 0.2 = 8.15 \ \mu\Omega
\]

(b.) The area or the source and drain are equal and are 9µm by 22µm or 198µm². The perimeter of the source and drain are \(2(9\mu m + 22\mu m)\) or 62µm. Therefore,

\[
C_{BD} = C_{BS} = 770 \times 10^{-6} \text{F/m}^2 \times 198 \times 10^{-12} \text{m}^2
\]

\[
+ 380 \times 10^{-12} \text{F/m} \times 62 \times 10^{-6} \text{m}
\]

\[
C_{BD} = C_{BS} = 152 \text{fF} + 24 \text{fF} = 176 \text{fF}
\]

(c.) The \(W = 22\mu m\) and the \(L = 2\mu m\).

(d.) The overlap capacitor is

\[
C_{GD} = 220 \times 10^{-12} \text{F/m} \times 22 \times 10^{-6} \text{m} = 4.8 \text{fF}
\]
Problem 3

A simple first-order filter shown is to be built with a polysilicon resistor and a MOS capacitor. The polysilicon resistor has a sheet resistance of 50 $\Omega$/sq. $\pm$ 30% and is 5$\mu$m wide. The MOS capacitor is 2fF/$\mu$m$^2$ $\pm$ 10%. The -3dB frequency of the lowpass filter is 1MHz. (a.) Choose the size of the resistor (the number of squares, $N$) to minimize the total area of the filter including both the resistor and the capacitor. Find the area of the resistor and the capacitor in $\mu$m$^2$ and their values. (b.) Using the worst-case tolerance of the resistor and capacitor, find the maximum and minimum -3dB frequencies.

Solution

(a.) Value of $R = 50 \ \Omega$/sq.$\times N$ sq.$ = 50N$  

Value of $C = 2fF/\mu m^2 \times AC \ \mu m^2 = 2AC$ fF

Area of $R = AR = 25 \mu m^2 \times N = 25N \ \mu m^2$  

Area of $C = AC$

Total Area $A_T = (25N + AC) \ \mu m^2$

We know that the $RC$ product is given as  

$RC = \frac{1}{2p \times 10^6} = (50N)(2AC \times 10^{-15}) = NAC \times 10^{-13}$  

$AC = \frac{1}{2p \times 10^{-7}N}$
Problem 3 - Continued

Thus, \( A_T = 25N + \frac{1}{2 \times 10^{-7}N} \)  \( \frac{dA_T}{dN} = 25 - \frac{1}{2 \times 10^{-7}N^2} = 0 \)

\[ N = \frac{1}{\sqrt{50 \times 10^{-7}}} = 252 \]

\( N = \frac{1}{\sqrt{50 \times 10^{-7}}} = 252 \)

\( A_{R} = 252 \times 25 \mu m^2 = 6308 \mu m^2 \) and \( A_{C} = 6308 \mu m^2 \)

Also, \( R_{poly} = R = 252 \times 50 = 12.6k\Omega \) and \( C_{MOS} = 6308 \mu m^2 \times 2fF/\mu m^2 = 12.6pF \)

(b.)

Maximum -3dB frequency = \( \frac{1}{2p(0.7)(12.6k\Omega)(0.9)(12.6pF)} = 1.6MHz \)

Minimum -3dB frequency = \( \frac{1}{2p(1.3)(12.6k\Omega)(1.1)(12.6pF)} = 0.7MHz \)
Problem 4

A CMOS amplifier is shown along with the top view of the circuit layout assuming a p-well CMOS technology. Find the values of the capacitors shown in the circuit if

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<th>Type</th>
<th>P-Channel</th>
<th>N-Channel</th>
<th>Units</th>
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<tr>
<td>CGDO</td>
<td>220</td>
<td>220</td>
<td>pF/m</td>
</tr>
<tr>
<td>CGSO</td>
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<td></td>
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<tr>
<td>CGBO</td>
<td>700</td>
<td>700</td>
<td>pF/m</td>
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<tr>
<td>CJ</td>
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<td>770</td>
<td>pF/m^2</td>
</tr>
<tr>
<td>CJSW</td>
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<td>380</td>
<td>pF/m</td>
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<td>MJ</td>
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<td>0.5</td>
<td></td>
</tr>
<tr>
<td>MJSW</td>
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<td></td>
</tr>
<tr>
<td>2</td>
<td>F</td>
<td></td>
<td>0.7</td>
</tr>
</tbody>
</table>

Based on an oxide thickness of 140 Å or Cox=24.7 pF/m^2.

Solution

\[ C_{gd1} = 220 \text{p} \times 10 \mu = 2.2 \text{fF} \]
\[ C_{gd2} = 220 \text{p} \times 20 \mu = 4.4 \text{fF} \]
Problem 4 - Continued

Next, we must find the area and perimeter of each drain.

AD1 = 60µm² & PD1 = 32µm
AD2 = 120µm² & PD2 = 52µm

\[
C_{bd1} = \frac{CJ \cdot AD1}{1 + \left(\frac{2.5V}{2|fF|}\right)MJ} + \frac{CJSW \cdot PD1}{1 + \left(\frac{2.5V}{2|fF|}\right)MJSW} = \frac{770 \times 10^{-6} \cdot 60 \times 10^{-12}}{1 + \left(\frac{2.5V}{0.8}\right)^{0.5}} + \frac{380 \times 10^{-12} \cdot 32 \times 10^{-6}}{1 + \left(\frac{2.5V}{0.8}\right)^{0.38}}
\]

\[C_{bd1} = 22.75fF + 7.10fF = 29.84fF\]

\[
C_{bd2} = \frac{CJ \cdot AD2}{1 + \left(\frac{2.5V}{2|fF|}\right)MJ} + \frac{CJSW \cdot PD2}{1 + \left(\frac{2.5V}{2|fF|}\right)MJSW} = \frac{560 \times 10^{-6} \cdot 120 \times 10^{-12}}{1 + \left(\frac{2.5V}{0.7}\right)^{0.5}} + \frac{350 \times 10^{-12} \cdot 52 \times 10^{-6}}{1 + \left(\frac{2.5V}{0.7}\right)^{0.35}}
\]

\[C_{bd2} = 31.43fF + 10.69fF = 42.12fF\]
Problem 5

A CMOS circuit is shown. Assume a p-well CMOS technology and draw the complete layout for the NMOS and PMOS transistors that has minimum rectangular area for the source and drain diffusions. Some pertinent design rules are listed below.

- DR1 = distance from the square contact to diffusion from polysilicon = 2µm
- DR2 = all contacts are to be square with a dimension of 2µm by 2µm
- DR3 = the overlap of the contact by the diffusion or poly = 2µm
- DR4 = min. separation between n+ diffusion and p-well = 2µm
- DR5 = minimum overlap of contact by metal = 1µm
- DR6 = poly must overlap the channel by 1µm

All metal widths are to be 4µm. Put as many contacts between the metal and diffusions as possible. Show the metal connections between transistors and indicate where metal goes for connections from transistors to external connections (vi and vo must be in metal). Use the indicated scheme below for identifying the various regions. If you wish to use colored pencil, use the scheme below or indicate which colors pertain to which region.
Problem 5 – Continued

Solution

Blue  Green  Black  Red  Orange  White
n+  p+  Metal  Poly  p-well  n-substrate

Fig. F99E1S1B
Problem 6

This problem consists of a number of short questions

1. What is the resistance of the drain if the sheet resistance of \( n^+ \) diffusion is \( 10 \ \Omega/\text{sq.} \)? What is the drain-bulk capacitance assuming \( V_{BD} = 0 \text{V} \) if bottom capacitance is \( 0.33 \text{pF/\mu m}^2 \) and the sidewall capacitance is \( 0.9 \text{fF/\mu m} \)?

\[
R_{n^+} = 10 \ \Omega/\text{sq.} \times \frac{8}{7} = 11.43
\]

\[
C_{BD} = 0.33 \text{pF/\mu m}^2 \times 70 \mu \text{m}^2 + 0.9 \text{fF/\mu m} \times 34 \mu \text{m} = 23.1 \text{fF} + 30.6 \text{fF} = 53.7 \text{fF}
\]

\[
\boxed{C_{BD} = 53.7 \text{fF}}
\]

2. What is the function of the field oxide (FOX) in a CMOS technology? The function of field oxide is to isolate the substrate from conductors on the surface.
Problem 6 – Continued

3. How are two BJT transistors fabricated in the same substrate electrically isolated from each other?
   
   Each BJT is fabricated in its own n-epitaxial region surrounded on all sides by p material. This pn junction is reversed biased to electrically isolate the two transistors.

4. List the 5 capacitances associated with the MOSFET operating in the saturation region and tell whether this capacitance is depletion or parallel plate or both.
   1.) Gate-drain which is parallel plate
   2.) Gate-source which is parallel plate
   3.) Bulk-drain which is depletion
   4.) Bulk-source which is depletion
   5.) Gate-bulk which is parallel plate
Problem 7

A top view of a CMOS push-pull amplifier is shown. Find the numerical value of all capacitances shown on the schematic. Assume that the dc value of the output is 2.5V and the MJ and MJSW is 0.5 for both transistors.
Problem 7 - Continued

Solution

M1: \( W_1 = 10\mu m, L_1 = 2\mu m, AS_1 = AD_1 = 6 \times 10 = 60\mu m^2, PS_1 = PD_1 = 32\mu m \)

\[
C_{GD1} = 10\mu m \cdot 0.45\mu m \cdot 0.7fF/\mu m^2 = 3.15fF
\]

\[
C_{BD1} = \frac{[60\mu m^2 \cdot 0.33fF/m^2 + 32\mu m \cdot 0.9fF/\mu m]}{\sqrt{1 + \frac{2.5}{0.6}}} = 21.38fF
\]

\[
C_{GS1} = 10\mu m \cdot 0.45\mu m \cdot 0.7fF/\mu m^2 + 0.67[20\mu m^2 \cdot 0.7fF/m^2] = 12.48fF
\]

M2: \( W_2 = 20\mu m, L_2 = 2\mu m, AS_2 = AD_2 = 6 \times 20 = 120\mu m^2, PS_2 = PD_2 = 52\mu m \)

\[
C_{GD2} = 20\mu m \cdot 0.6\mu m \cdot 0.7fF/\mu m^2 = 8.4fF
\]

\[
C_{BD2} = \frac{[120\mu m^2 \cdot 0.38fF/m^2 + 52\mu m \cdot 1fF/\mu m]}{\sqrt{1 + \frac{2.5}{0.6}}} = 42.94fF
\]

\[
C_{GS2} = 20\mu m \cdot 0.6\mu m \cdot 0.7fF/\mu m^2 + 0.67[40\mu m^2 \cdot 0.7fF/m^2] = 27fF
\]
Problem 8  This problem consists of a number of short questions

1. List three functions of polysilicon.
   (1) Gate of a MOS transistor
   (2) Ohmic connection between two points
   (3) Resistor
   (4) Capacitor plate

2. In a CMOS technology, list three functions for the n⁺ or p⁺ diffusions.
   (1) They can form the source or drain of a MOSFET
   (2) They are used to make an ohmic contact with metal
   (3) They can be used as a resistor
   (4) Capacitor plate

3. Nitride is only used to define the active areas of transistors. True___ or False_X

4. How are two NMOS transistors fabricated in the same substrate electrically isolated from each other?
   They are fabricated in an oppositely doped substrate so that they can be reverse biased and thus isolated from the substrate and from each other.

5. What is the purpose of masks in an integrated circuit fabrication process?
   To allow selective processing of an area of a wafer.
Problem 9

A CMOS layout is shown. (a.) Draw the schematic corresponding to this layout. What is this circuit? (b.) Find the value of $CBD$, $CBS$, $CGD$ and $CGS$ of all transistors. Assume zero-bias for any voltage dependent capacitors and that all transistors are saturated.

**Solution**

(a.) The schematic for this circuit is shown. The circuit is a simple NMOS current mirror.

(b.) There are two transistors that are identical. The drain areas and peripheries are:

$$AD = 5 \times 13 = 65\mu m^2, \ PD = 10 + 26 = 36\mu m$$

The sources are shared. We will simply divide the bulk-source capacitances by two, using the above area and periphery for the source.

$$CBD = 0.33fF/\mu m^2 \times 65\mu m^2 + 0.9fF/\mu m \times 36\mu m = 21.4fF + 32.4fF = 53.85fF$$

$$CBS = 0.5 \times CBD = 26.9fF \quad CGD = COL = 13\mu mx0.45\mu mx0.7fF/\mu m^2 = 4.1fF$$

$$CGS = COL + 0.67 \cdot W \cdot L \cdot Cox = COL + 0.67 \times 13\mu mx2\mu mx0.7fF/\mu m^2 = 4.1fF + 12.1fF = 16.2fF$$