GEORGIA INSTITUTE OF TECHNOLOGY  
School of Electrical and Computer Engineering  

LCE 3050-B  
Fall 2001  

Second Test  
October 24, 2001  

General Instructions:

1. Write on one side of the paper. (1 Pt.)

2. Put answers to all questions in the spaces provided on the test. (1 Pt.)

3. Show all work for full credit on questions requiring calculations. No credit will be given for answers alone, without supporting work.

4. Problems and questions are weighted as indicated. The maximum score is 100 points.

5. If you need more paper (provided in class), unstaple test and, when finished, arrange the test in order. Place the extra pages with supporting work in the test behind the page where the problem appears. Staple the entire test together so that there are no loose pages. (1 Pt.)

TEST SCORE: ____________________________ / 100

I certify that I have neither given nor received any assistance while taking this test from anyone.

____________________________________ (Signature) (1 Pt.)

☐ Place a check mark in the box if you observed any suspicious actions while taking this test.
**Formula Sheet:** Equations/Constants that you may, or may not, need are listed below:

\[ K' = 50 \ \mu A/V^2 \] (unless otherwise stated in the problem) and \[ K_n = K' L / W \]

\[ I_{DS} = (K_n/2) [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2] \]

\[ \lambda = 0.01 \ V^{-1} \] (unless otherwise stated in the problem)

\[ I_{DS} = (K_n/2) (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS}) \]

\[ V_{gs} < 0.2(V_{GS} - V_{TN}) \rightarrow \text{small signal requirement} \]

\[ r_{n-MOS} = 1 / (\lambda V_{DS}) \]

\[ g_{m-MOS} = \sqrt{2(1+k)nK_n} \]

\[ V_{ds-sat} = \sqrt{2I_{DS}/K_n} \]

\[ g_{mb-MOS} = n g_{m-MOS} \]

\[ \eta = \gamma / 2 \sqrt{2(2\varphi_T - V_{BS})} \]

\[ V_{TO} = 0.7 \ V \] (unless otherwise stated in the problem)

\[ \gamma = 0.5 \ V^{1/2} \] (unless otherwise stated in the problem)

\[ 2\varphi_T = 0.6 \ V \] (unless otherwise stated in the problem)

\[ V_{TN} = V_{TO} + \gamma \left[ \sqrt{2(2\varphi_T - V_{BS})} - \sqrt{2\varphi_T} \right] \]

\[ V_t = kT/q = 26 \text{ mV} \text{ and } I_S = 1E-15 \ A \] (unless otherwise stated in the problem)

\[ I_D = I_S \left[ \exp(V_{D}/V_t) - 1 \right] \]

\[ V_A = 100 \ V \] (unless otherwise stated in the problem)

\[ I_{CE} = I_S \left[ \exp(V_{BE}/V_t) - 1 \right] \left[ 1 + V_{CE}/V_A \right] \]

\[ r_{n-NPN} = V_A / I_{CE} \]

\[ g_{m-NPN} = I_{CE}/V_t \]

\[ V_{be} < 5 \text{ mV} \rightarrow \text{small signal requirement} \]

\[ \beta_F = 50 \] (unless otherwise stated in the problem)
Problem 1 – (24 Points)

a) What type of amplifier configuration is Stage 1? \( CE \) (2 pts)
b) What type of amplifier configuration is Stage 2? \( CS \) (2 pts)
c) What type of amplifier configuration is Stage 3? \( CE/\text{Darlington} / \text{V-Follower} \) (2 pts)
d) What is the purpose of resistor \( r_{s2} \)? \( \text{bypassing} \Rightarrow I_{eb} \) (2 pts)
e) What is the purpose of \( r_{e1} \)? \( \text{ac shunt/bypass} \Rightarrow \text{gain} \) (2 pts)
f) What is the purpose of \( r_{c1} \)? \( \text{ac coupling} \Rightarrow \text{dc block & ac pass} \) (2 pts)
g) Which stage(s) provide 0 degrees of phase shift? 3 (2 pts)
h) Which stage(s) provide 180 degrees of phase shift? 1, 2 (4 pts)
i) What happens to the ac input resistance of Stage 2 \( (r_{m2}) \) if \( cs2 \) were to be removed? \( \text{Nothing} \) (2 pts)
j) Which stage(s) are more likely to provide significant voltage gain (e.g., \( |A_v| \gg 1 \))?

1, 2 or 1 (2 pts)
k) Which bipolar stage will more than likely provide the most current gain? 3 (2 pts)
Problem 2 – (72 Points)

Answer the questions given based on the schematic shown below and the edited output Spice file printed on a subsequent page. Note that most of the pertinent device parameters are contained within the Spice file ($\beta_r$, $V_A$, $V_T$, etc.) and will override the assumptions made in the formula sheet. Ensure that proper signs and dimensional units are given in your answers. If you do not know the answer to one part, and need it for a subsequent part, assume a reasonable value, state it, and proceed. For your analysis, assume that the values of the capacitors are arbitrarily large. For questions asking “What,” you may simply state the equation and answer, if you know it (without derivation). However, for questions with “Derive,” you are expected to derive the equation (draw the pertinent equivalent circuit, if appropriate).

![Schematic Diagram]

a) What is the transconductance of $q_{n1}$ ($g_{m-n1}$) – not the transconductance of Stage 1

$$g_{m-n1} = \frac{I_{ce1}}{V_{te}} = \frac{1.4}{26 \text{ mV}} = 56 \text{ mS}$$

(5 pts)

b) What is the transconductance of $mp2$ ($g_{m-p2}$) – not the transconductance of Stage 2

$$g_{m-p2} = \frac{\sqrt{2 I_{be2} k' (10)}}{\sqrt{2 (120 \text{ mV}) (20 \text{ mV}) (10)}} = 219 \text{ mS}$$

(5 pts)

c) What is the output resistance of $q_{n1}$ ($r_{on1}$)?

$$r_{on1} = \frac{V_A}{I_{ce1}} = \frac{100}{1.4 \text{ mS}} = 69 \text{ K}\Omega$$

(5 pts)

d) What is the output resistance of $mp2$ ($r_{on2}$)?

$$r_{on2} = \frac{1}{\lambda} \frac{1}{I_{be2}} = \frac{1}{(120 \text{ mV}) (120 \text{ mV})}$$

(5 pts)
Problem 2 – (Continued)

e) Derive the output resistance seen at the emitter of qn31 (R_{out-31})? – Neglect \( r_{p32} \) & \( r_{np2} \)
(Hint: Resolve \( V_{iex} \) and \( I_{iex} \) in terms of \( i_b \) and \( \beta \))

\[
\begin{align*}
\frac{V_{\text{ex}+}}{I_{\text{ex}+}} &= R_{\text{out}} = \frac{f_{b} (f_{b} + f_{T31})}{1 + f_{b}} = \frac{f_{b} + f_{T31}}{1 + f_{b}} \frac{I_{\text{ex}+}}{V_{E}} \\
\approx \frac{f_{b} + 20K \beta}{\beta} = 20K \frac{\beta}{\beta} = 20K \frac{100}{100}
\end{align*}
\]

f) What is the ac voltage gain of Stage 1? – Neglect \( r_{e31} \)

\[
-3 \cdot \frac{V_{E}}{V_{E}} = -263
\]

(5 pts)

g) Derive the ac voltage gain of Stage 2, if cs2 were to be removed? – Neglect \( r_{p32} \) & \( R_{in-31} \)

\[
\begin{align*}
A_{V} &= -g_{m} R_{out} = -16 \cdot 10^{-3} (30K) = -0.48 \frac{V}{V} \\
V_{o} &= \left. g_{m} V_{G} \right|_{V_{G}=0} = \frac{-g_{m} V_{G}}{V_{G}} = \frac{-3V_{G}}{V_{G}} = -3
\end{align*}
\]

(12 pts)
Problem 2 – (Continued)

b) Derive the ac voltage gain of Stage 3 (including rl)? Neglect \( r_{o31} \) & \( r_{o32} \) \( + \) \( \frac{1}{V/V} \) (10 pts)

(Hint: Resolve \( V_o \) and \( V_i \) in terms of \( i_b \))

\[
A_v = \frac{V_o}{V_i} = \frac{\beta_2(1+\beta_1)(1+\beta_2) \cdot V_{re2}}{\beta_2(1+\beta_1) + \beta_2(1+\beta_2) \cdot V_{re2}}
\]

\[
\beta_2 \cdot \frac{V_{re2}}{\beta_1} \cdot \frac{100(26m)}{100} = 210K \rightarrow \beta_1 \cdot r_{3132} = 18.6K
\]

\[
\frac{V_{re2}}{\beta_1} \cdot \frac{100(26m)}{100} = 1.8K \rightarrow \beta_2 \cdot r_{3132} = 18.6K
\]

i) What is the ac voltage gain of the whole circuit if the gain of the second stage is assumed to be -6.57 \( V/V \)?

\[
A_1 \cdot A_2 \cdot A_3 = (-2.63)(-6.57)(+1) = 17.3 K \cdot \frac{V}{V} \quad (5 \text{ pts})
\]

j) Derive the output resistance seen down into the collector of qn1 (R_o), if ce1 were to be removed?

\[
R_o = \frac{V_o}{I_o} = \frac{\left[\beta_2 + (R_{m1} + g_m) \cdot r_o \cdot \frac{V_{re1}}{\beta_2}\right]}{I_o}
\]

\[
= \frac{\left\{\beta_2 + (\beta_2 \cdot g_m \cdot r_{e1} / g_m) \cdot r_o \cdot V_{re1} + \beta_2 \cdot (r_{m1} / g_m) \cdot V_{re1}\right\}}{I_o}
\]

\[
= \frac{V_{m1} / g_m \cdot V_{re1} + r_o \cdot (1 + g_m \cdot r_{m1} / g_m)}{1.6K}
\]

\[
= 3.35 \text{ M } \Omega
\]
Problem 2 – (Continued)

Spice Output File

vi vi 0 de 0 ac 1
*setup
ci vi bi 10u
vdd vdd 0 de 15
r01 bi 0 22k
r02 vdd bi 75k
q11 ci bl e1 npna
.model npna npna s=1e-15 bf=100 va=100
re1 ci 0 1.6k
ci1 e1 0 10u
ci1 vdd ci 4.7k
mp2 d2 ci s2 x2 proac w=10u l=1u
.model proac proac vo=1 k=20u lambda=0.01
rs2 vdd s2 50k
es2 s2 vdd 10u
rd2 d2 0 30k
q311 vdd d2 e31 npna
q32 vdd e31 e32 npna
re3 e32 0 1.6k
c e32 vo 10u
* prob

end

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

( b1 ) 3.0935 ( c1 ) 8.1895 ( d2 ) 3.5828 ( e1 ) 2.3405

( s2 ) 8.2582 ( vi ) 0.0000 ( vo ) 0.0000 ( e31 ) 2.9844

( e32 ) 2.2640 ( vdd ) 15.0000

**** BIPOLAR JUNCTION TRANSISTORS

NAME q11 q311 q32
MODEL npna npna npna
IB 1.38E-05 1.17E-07 1.22E-05
IC 1.43E-03 1.24E-05 1.40E-03
VBE 7.24E-01 5.98E-01 7.20E-01
VBC -5.12E-01 -1.14E-01 -1.20E-01
VCH 5.85E-09 1.20E-01 1.27E-01

**** MOSFETS

NAME mp2
MODEL proac
ID -1.20E-04
VGS -6.80E-02
VDS -4.68E-02
VBS 0.00E+00
VTH 1.00E+00
Extra Credit – (5 Points)

If you wanted to increase the input resistance ($R_{in}$) of the whole circuit, how would you change the first stage (only draw the circuit diagram and explain – no derivations required)?

![Circuit Diagram]

- **By replacing** $g_{m1}$ with $m_{n1}$
- **Since** $g_{0} = 0$ :: $R_{in} = \frac{1}{g_{m1}}$ **or** $\frac{1}{R_{ GS1}}$
- Which can be designed to be large

- **Or**
- **Remove** $C_{eb}$ and **use** same circuit but decrease the current through $g_{m1}$ (since $R_{in} \approx \frac{R}{g_{m}} = \frac{R}{I_{C}}$)
- **By increasing** the value of $R_{in}$