GEORGIA INSTITUTE OF TECHNOLOGY
School of Electrical and Computer Engineering

ECE 3040E **MICROELECTRONIC CIRCUITS** **Spring 2003**

INSTRUCTOR:	Dr. Gabriel A. Rincón-Mora Office: Van Leer, Room E-296-D Office phone: (404) 385-2768, Secretary: (404) 894-2973 E-mail: rincon-mora@ece.gatech.edu
TIME & LOCATION:	Monday/Wednesday/Friday: 2:05 – 2:55 p.m., Van Leer: C-456 Thursday: 2:05 – 2:55 p.m., Van Leer: C-456
OFFICE HOURS:	An RA (Susanta Sengupta - ssgupta@ece.gatech.edu) will hold office hours in Van Leer 308 on: Monday: 11:00 a.m. – 12:00 p.m. Tuesday: 11:00 a.m. – 12:00 p.m. Wednesday: 11:00 a.m. – 12:00 p.m. E-mail RA or Instructor for special requests
TEXTS:	***Semiconductor Device Fundamentals*** by R.F. Pierret, Addison-Wesley Publishing Co., 1996, ISBN 0-201-54393-1. ***Microelectronic Circuit Design*** by R. C. Jaeger, McGraw Hill, 1997, ISBN 0-07-032482-4.
PREREQUISITE:	ECE 2030, ECE 2040, and CHEM 1310, Or CHEM 1101, Or CHEM 1102, Or CHEM 1211, Or CHEM 12X1.
REFERENCES:	Some general purpose reference book describing SPICE and/or PSpice is strongly recommended. One such book is: ***Schematic Capture Using MicroSim PSpice for Windows 95/98/NT*** by M.E. Herniter, Prentice-Hall, 2000, ISBN: 0-13-081404-0.
PSPICE:	The educational version of PSpice for the PC is free and can be downloaded from http://www.cadencepcb.com/products/downloads/PSpicestudent/default.asp
WWW SUPPLEMENT:	http://users.ece.gatech.edu/rincon-mora/classes/resources.htm

COURSE OBJECTIVES

ECE 3040 introduces the fundamental concepts of microelectronic (semiconductor) materials, devices, and circuits. It also provides the foundation for the Integrated Circuit (IC) and Very Large Scale Integration (VLSI) design courses that follow in the sequence. In this course, you will learn the basic theory behind non-linear circuit elements, such as diodes, Bipolar Junction Transistors (BJT), and Field Effect Transistors (FET). The class will cover how the devices

operate, how they are built, and how they are modeled. Ultimately, these concepts will then be used to design basic analog and digital circuit building blocks, from diode rectifiers, regulators, and amplifiers to digital gates and memory cells. Intuitive understanding and real-life applications will be emphasized throughout the course.

EVALUATION

Course Grade Composition

Three 1-hour tests during the semester	60%
Homework problems	10%
Final Examination	25%
Professionalism	5%

The professionalism portion of your grade will basically depend on your adherence to the course policies outlined in this document as well as the ethical standards of the school and Georgia Tech at large. Your course grade will be evaluated on the basis of your performance relative to the rest of the class and upon what I consider to be good, passable, and unsatisfactory work.

Important Dates:

First day of classes	January 6, 2003 (Friday)
Official Holiday	January 20, 2003 (Monday)
Last day to drop a course	February 14, 2003 (Friday)
Spring Break	March 3 – 7, 2003 (Monday – Friday)
Last day of classes	April 25, 2003 (Friday)

Tentative Test Dates

1st Test	January 30, 2003 (Thursday)
2nd Test	February 27, 2003 (Thursday)
3rd Test	April 3, 2003 (Thursday)
Final Exam	May 1, 2003 (Thursday: 11:30 a.m. – 2:20 p.m.)

All tests will be closed textbook and notes. The bell will mark both the beginning and the end of the exam. Everybody must remain seated with their pencils down when the time period ends until otherwise instructed. All work must stop by the onset of the closing bell. "Make-up" tests are discouraged; in no case will a "make-up" test be given unless you have obtained approval from the instructor prior to the announced time of the test. Test grades become final one week after they are returned. If a question arises within a week, a note is to be placed on the front of the exam to indicate and explain the concern. I will then review the whole exam, for the issue in question and other possible grading errors –good or bad–, and return it within a week. Calculators cannot be used in the programmable mode during the tests or the final exam.

Reading Assignments: Motivated students will have read the sections recommended in the Syllabus, depending on which topic we are covering at the time, prior to attending class. Additional reading and handouts may be assigned in class. Reviewing the examples included in the text is excellent preparation for the tests and homework, as well as the links provided through the webpage for prior course material -homework and exams-.

Homework Problems: Homework problems are assigned for grading and as a study guide. Mature students will recognize the value of the homework as a guide for reinforcing class and text topics and as a potential source of test questions. Collaboration between students is allowed, and encouraged. However, the homework solution to be turned in must be unique. If two solutions are identical, one score will be assigned and it will be shared among the students with identical solutions (e.g., if two identical solutions earned 8 out of 8 points each, both students will earn a total of 8 points, 4 each). Late homework will be accepted with a 20% per day late penalty (including weekends) until the graded assignment is returned in class. Homework should be collected within one week of being graded. I will provide assistance concerning the solution to these and other problems in direct proportion to the written efforts you demonstrate for your own attempts toward the solution.

Final Examination: A final exam will be required of all students, including degree candidates.

Attendance: Strongly encouraged. Each student is responsible for all assignments, announcements, and material covered in each class. I will start and end class as close to the ringing of the school bell as possible. The other members of the class and I will appreciate and expect your punctual arrival.

Smoking, eating, and drinking: Prohibited in the classroom by ECE School rules.

ACADEMIC HONESTY

Cheating and other forms of academic dishonesty are on the rise nationally. Georgia Tech has specific rules regarding academic misconduct as well as an Academic Honor Code, which are described on the web at http://www.deanofstudents.gatech.edu/Policy/code1.html. Your role as a Georgia Tech student requires you to know and follow these rules. My role as your instructor requires that I evaluate each student individually and as fairly as humanly possible. I will not tolerate academic dishonesty in this class. I expect your cooperation in reporting any suspicious act relating to academic misconduct. As such, I will follow the guidelines, which states that I should "*report (all) instances of academic dishonesty to the Office of the Dean of Students"*.

SPECIAL CIRCUMSTANCES

If a student has a disability that may require special accommodations, please make an appointment with the ADAPTS office (http://www.adapts.gatech.edu/) to discuss any special needs as well as schedule an appointment with me.

HOMEWORK GUIDELINES

The following guidelines are to be followed so that your written homework can be evaluated as accurately and as easily as possible.

- Use a cover sheet on which you clearly print your full name, the date, the course number, and the homework assignment number.
- Number each problem at a position on the page where the number will not be covered by a staple. Label each part of the problem with the complete number –number and section, e.g., 3(a), 4(b), etc.–.
- Clearly label the circuit diagrams with all the pertinent voltages and currents.

- The methods you used to obtain the numerical values must be clear from your solution. Numerical answers must contain proper dimensional units wherever appropriate.
- If you must submit out-of-order work, clearly indicate this at the appropriate point in your work, and state where the continuation work can be found. For example, suppose you accidentally omit part (c) from Problem 1 when you first write up your solutions. You may later add part 1(c), out of order, if you clearly indicate at the end of part 1(b) where part 1(c) can be found.
- Clearly mark all answers by putting a box around them.
- If you do not complete a problem, or any part of a problem, write the word "end" at the point where you stopped, and underline it. This word will indicate that the answer will not be found elsewhere in your paper.

The following extra items are required on homework problems that demand SPICE simulations:

- A circuit diagram with SPICE nodes labeled, numbered or named.
- The input control file or files you used to generate your SPICE results.
- Edited and highlighted SPICE results which support your numerical results. SPICE results that are unedited and not annotated will not be graded.

Tentative Course Topics:

Topics	***Suggested/Additional Reading P-Pierret J-Jaeger***
Course Policies Course Introduction Semiconductor Materials Crystal Structure Semiconductor Models Carrier Properties	P 1.1, 1.2, 2.2, 2.3
State and Carrier Distributions Equilibrium Carrier Concentrations Drift	P 2.4, 2.5, 3.1
Diffusion Generation/Recombination	P 3.2, 3.3
Generation/Recombination Equations of State	P 3.3, 3.4
Intro PN Junctions PN Electrostatics	P 5.1, 5.2
Ideal Diode Diode Large-Signal Model Diode Circuit Analysis Diode Spice Model	P 6.1 J 3.9
Diode Applications Diode Breakdown Diode Small-Signal Model Introduction to BJTs BJT Physics	J 3.12, 3.7, 13.4 P 9.2, 10.4, 10.5, 11.1
BJT Large-Signal Model	P 11.1
BJT Small-Signal Model BJT Spice Model	J 13.5
MOS Capacitor MOSFET Basics MOSFET Device Physics	P 16.2, 16.3, 17.1, 17.2
MOSFET Small-Signal Model MOSFET Spice Model Single Stage Amplifiers Common Emitter Common Source	J 13.6, 13.7, 13.9, 13.10, 13.11
Common Collector/Drain	J 14.1, 14.3
Common Base/Gate Differential Amplifier	J 14.1, 14.4, 15.3
Operational Amplifier 1st order Op-Amp Circuits Non-Ideal Op Amps & Active Filters	J 12.1, 12.2, 12.3, 12.5
Logic Gates and Levels Dynamic Response	J 6.1, 6.2, 6.3, 6.4, 7.1, 7.2, 7.3, 7.4, 8.1, 8.2, 8.3, 8.4,

Boolean Algebra Inverters Logic Gates CMOS Gates	8.5