MOSFET SPICE Model

- SPICE models the drain current (I_{DS}) of an n-channel MOSFET using:

Cut-off: $(V_{GS} \leq V_{TH})$

$I_{DS} = 0$

Linear: $(0 \leq V_{DS} \leq V_{GS} - V_{TH})$

$$I_{DS} = \frac{KP}{2}\left(\frac{W}{L_{eff}}\right)V_{DS}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}](1 + LAMBDA \cdot V_{DS})$$

Saturation: $(0 \leq V_{GS} - V_{TH} \leq V_{DS})$

$$I_{DS} = \frac{KP}{2}\left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{TH})^2(1 + LAMBDA \cdot V_{DS})$$

MOSFET SPICE Model

- Threshold voltage is given by:

$$V_{TH} = V_{TO} + GAMMA(\sqrt{2PHI - V_{BS}} - \sqrt{2PHI})$$

- SPICE definition for channel length (L_{eff}):

$$L_{eff} = L - 2LD$$

where: L = length of the polysilicon gate
LD = gate overlap of the source and drain

MOSFET SPICE Model

- n-channel MOSFET is defined by the SPICE statement:

M*name D G S B MODname* **L**=_ **W**=_ **AD**=_ **AS**=_ **PD**=_ **PS**=_ **NRD**=_ **NRS**=_

where: name = name of the device (up to 7 characters)

D, G, S, B = drain, gate, source, and substrate node numbers

MODname = model name for the device (see below)

L = polysilicon gate length (see figure)

W = polysilicon gate width (see figure)

AD = drain area (see figure)

AS = source area (see figure)

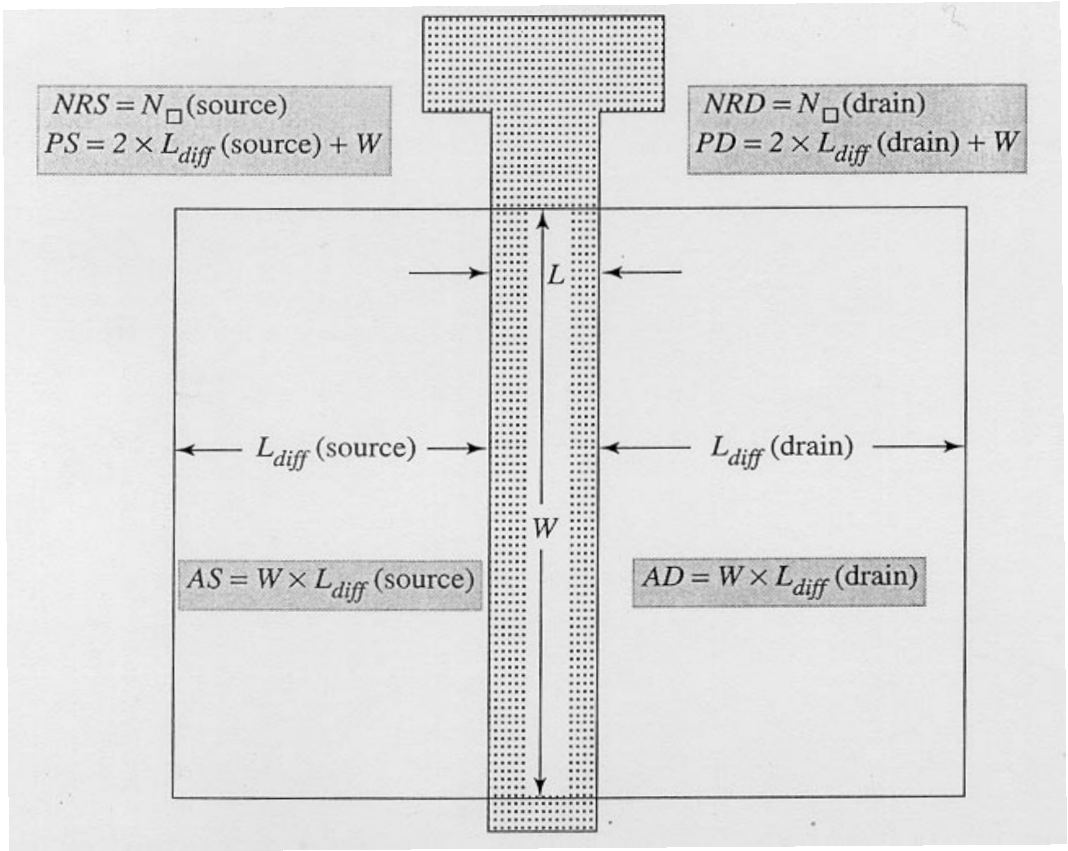
PD = perimeter of drain diffusion (not including edge under gate)

PS = perimeter of source diffusion (not including edge under gate)

MOSFET SPICE Model

NRD = number of “squares” in drain diffusion

NRS = number of “squares” in source diffusion



MOSFET SPICE Model

- MOSFET model statement is:

.MODEL *MODname* **xMOS VTO=_ KP=_ GAMMA=_ PHI=_ LAMBDA=_ RD=_ RS=_ RSH=_ CBD=_ CBS=_ CJ=_ MJ=_ CJSW=_ MJSW=_ PB=_ IS=_ CGDO=_ CGSO=_ CGBO=_ TOX=_ LD=_**

where: x = N (for NMOS) or P (for PMOS)

CGDO, CGSO, CGBO = gate overlap capacitance with drain, source, body

RD = drain contact resistance (Ω)

RS = source contact resistance (Ω)

RSH = sheet resistance of drain/source diffusions

(Ω/square; NRD and NRS must be specified)

IS = diode saturation current for pn junctions at the drain and source

MOSFET SPICE Model

- MOSFET model statement (cont.):

CBD = zero-bias drain-substrate capacitance (F)

$$C_{BD}(V_{BD}) = \frac{C_{BD}}{(1 - V_{BD}/PB)^{MJ}}$$

CBS = zero-bias source-substrate capacitance (F)

$$C_{BS}(V_{BS}) = \frac{C_{BS}}{(1 - V_{BS}/PB)^{MJ}}$$

PB = built-in potential for the substrate junctions (V)

MJ = bulk junction grading coefficient

MOSFET SPICE Model

- More accurate simulations incorporate both the planar junction capacitance and perimeter (sidewall) capacitances as:

$$C_{BD}(V_{BD}) = \frac{CJ \cdot AD}{(1 - V_{BD}/PB)^{MJ}} + \frac{CJSW \cdot PD}{(1 - V_{BD}/PB)^{MJSW}}$$

$$C_{BS}(V_{BS}) = \frac{CJ \cdot AS}{(1 - V_{BS}/PB)^{MJ}} + \frac{CJSW \cdot PS}{(1 - V_{BS}/PB)^{MJSW}}$$

where: CJ = zero-bias planar substrate junction capacitance (F/m^2)

CJSW = zero-bias planar sidewall junction capacitance (F/m)

MJSW = sidewall junction grading coefficient

MOSFET SPICE Model

- These and remaining nMOS model parameters:

Parameter	Symbol	SPICE name	Units	Standard Value
Channel length	L	LEFF	m	
Polysilicon gate length	L_{gate}	L	m	
Gate-source overlap	L_D	LD	m	0
Transconductance parameter	$\overline{\mu}_n C_{ox}'$	KP	A/V^2	50×10^{-6}
Threshold voltage	V_{T0}	VTO	V	1.0
Channel length modulation parameter	λ	LAMBDA	V^{-1}	0.1/L (L in μm)
Backgate effect parameter	γ	GAMMA	$V^{1/2}$	0.6
Bulk potential	ϕ_F	PHI	V	0.8

Parameter	Symbol	SPICE name	Units	Standard Value
Gate oxide thickness	t_{ox}	TOX	ang-stroms	150
Gate-drain overlap capacitance	C_{gd}	CGDO	F/m	5×10^{-10}
Gate-source overlap capacitance	C_{gs}	CGSO	F/m	5×10^{-10}
Zero-bias planar substrate depletion capacitance	C_{j0}	CJ	F/m^2	10^{-4}
Zero-bias sidewall substrate depletion capacitance		CJSW	F/m	5×10^{-10}
Substrate junction potential	ϕ_B	PB	V	0.95
Planar substrate junction grading coefficient		MJ	-	0.5
Sidewall substrate junction grading coefficient		MJSW	-	0.33

```
ID vs VDS for NMOS
* (W/L = 1)
M1 D G S B NMOS2 (W=1u L=1u)
VG G 0 2
VD D 0 5
VS S 0 0
VB B 0 0
*
.MODEL NMOS2 NMOS(VTO=1.0 KP=25E-6 LAMBDA=0.0)
.OP
.DC VDS 0 12 0.2 VG 1 4 0.25
.PRINT DC ID(M1)
.PROBE
.END
```