MOSFET SPICE Model

- SPICE models the drain current ($I_{DS}$) of an n-channel MOSFET using:

  **Cut-off:** ($V_{GS} \leq V_{TH}$)
  
  $$I_{DS} = 0$$

  **Linear:** ($0 \leq V_{DS} \leq V_{GS} - V_{TH}$)
  
  $$I_{DS} = \frac{KP}{2}\left(\frac{W}{L_{eff}}\right)V_{DS}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}\right](1 + \text{LAMBDA} \cdot V_{DS})$$

  **Saturation:** ($0 \leq V_{GS} - V_{TH} \leq V_{DS}$)
  
  $$I_{DS} = \frac{KP}{2}\left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{TH})^2(1 + \text{LAMBDA} \cdot V_{DS})$$
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- Threshold voltage is given by:

\[ V_{TH} = V_{TO} + \text{GAMMA}(\sqrt{2\text{PHI}} - V_{BS} - \sqrt{2\text{PHI}}) \]

- SPICE definition for channel length (\( L_{\text{eff}} \)):

\[ L_{\text{eff}} = L - 2LD \]

where:
- \( L \) = length of the polysilicon gate
- \( LD \) = gate overlap of the source and drain
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- n-channel MOSFET is defined by the SPICE statement:

\[ M_{\text{name}} D G S B MOD_{\text{name}} L=_ W=_ AD=_ AS=_ PD=_ PS=_ NRD=_ NRS=_ \]

where: name = name of the device (up to 7 characters)

D, G, S, B = drain, gate, source, and substrate node numbers

MODname = model name for the device (see below)

L = polysilicon gate length (see figure)

W = polysilicon gate width (see figure)

AD = drain area (see figure)

AS = source area (see figure)

PD = perimeter of drain diffusion (not including edge under gate)

PS = perimeter of source diffusion (not including edge under gate)
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NRD = number of “squares” in drain diffusion

NRS = number of “squares” in source diffusion

\[
\begin{align*}
  NRS &= N_{\square} \text{(source)} \\
  PS &= 2 \times L_{\text{diff}} \text{(source)} + W \\
  NRD &= N_{\square} \text{(drain)} \\
  PD &= 2 \times L_{\text{diff}} \text{(drain)} + W
\end{align*}
\]
MOSFET SPICE Model

- MOSFET model statement is:

`.MODEL MODname xMOS VTO= KP= GAMMA= PHI= LAMBDA= RD= RS= RSH= CBD= CBS= CJ= MJ= CJSW= MJSW= PB= IS= CGDO= CGSO= CGBO= TOX= LD=`

where:  
x = N (for NMOS) or P (for PMOS)

CGDO, CGSO, CGBO = gate overlap capacitance with drain, source, body

RD = drain contact resistance (Ω)

RS = source contact resistance (Ω)

RSH = sheet resistance of drain/source diffusions

(Ω/square; NRD and NRS must be specified)

IS = diode saturation current for pn junctions at the drain and source
MOSFET SPICE Model

- MOSFET model statement (cont.):

  CBD = zero-bias drain-substrate capacitance (F)

  \[ C_{BD}(V_{BD}) = \frac{C_{BD}}{(1 - V_{BD}/PB)^{MJ}} \]

  CBS = zero-bias source-substrate capacitance (F)

  \[ C_{BS}(V_{BS}) = \frac{C_{BS}}{(1 - V_{BS}/PB)^{MJ}} \]

  PB = built-in potential for the substrate junctions (V)

  MJ = bulk junction grading coefficient
MOSFET SPICE Model

More accurate simulations incorporate both the planar junction capacitance and perimeter (sidewall) capacitances as:

\[
C_{BD}(V_{BD}) = \frac{C_J \cdot AD}{(1 - V_{BD}/PB)^{MJ}} + \frac{C_{JSW} \cdot PD}{(1 - V_{BD}/PB)^{MJSW}}
\]

\[
C_{BS}(V_{BS}) = \frac{C_J \cdot AS}{(1 - V_{BS}/PB)^{MJ}} + \frac{C_{JSW} \cdot PS}{(1 - V_{BS}/PB)^{MJSW}}
\]

where:
- \(C_J\) = zero-bias planar substrate junction capacitance (F/m²)
- \(C_{JSW}\) = zero-bias planar sidewall junction capacitance (F/m)
- \(MJSW\) = sidewall junction grading coefficient
MOSFET SPICE Model

- These and remaining nMOS model parameters:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>SPICE name</th>
<th>Units</th>
<th>Standard Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length</td>
<td>$L$</td>
<td>LEFF</td>
<td>m</td>
<td></td>
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<tr>
<td>Polysilicon gate length</td>
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<td>m</td>
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<td>Gate-source overlap</td>
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<td>Transconductance parameter</td>
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<td>VTO</td>
<td>V</td>
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<tr>
<td>Channel length modulation parameter</td>
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<td>LAMBDA</td>
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<tr>
<td>Backgate effect parameter</td>
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<td>Bulk potential</td>
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<td>Parameter</td>
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<td>F/m$^2$</td>
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<td>Zero-bias sidewall substrate depletion capacitance</td>
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<tr>
<td>Sidewall substrate junction grading coefficient</td>
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ID vs VDS for NMOS
* (W/L = 1)
M1 D G S 8 NMOS2 (W=1u L=1u)
VG G 0 2
VD D 0 5
VS S 0 0
VB B 0 0
*
.MODEL NMOS2 NMOS(VTO=1.0 KP=25E-6 LAMBDA=0.0)
.OP
.DC VDS 0 12 0.2 VG 1 4 0.25
.PRINT DC ID(M1)
.PROBE
.END