

# *MOSFETs*

*By*

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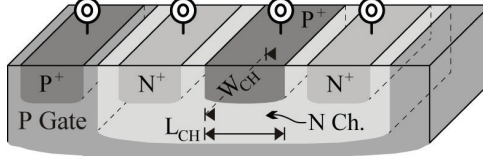
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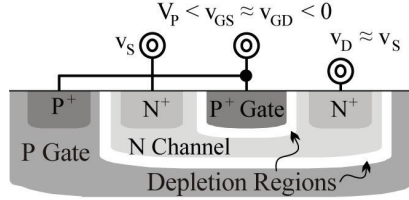
length  $L_{CH}$  or  $L$  and width  $W_{CH}$  or  $W$  are the longitudinal length and width of the overlapping  $P^+$ – $N$  channel– $P$  gate layers. The Ohmic surface contact of the bottom gate is another highly doped  $P^+$  region.



**Fig. 1.** N-channel JFET structure.

### A. Triode

The NJFET is basically an  $N$  resistor pinched by  $P$  regions. The geometry and doping concentration of the channel set baseline *channel resistance*  $R_{CH}$ .  $R_{CH}$  climbs as the depletion space against the top and bottom  $P$  regions in Fig. 2 expand to squeeze the channel. These  $P$  regions are the *gates*  $v_G$  of the JFET because their voltage adjusts  $R_{CH}$ .



**Fig. 2.** Uniformly biased N-channel JFET in triode.

$R_{CH}$  is high when  $L$  is long,  $W$  is narrow, and *baseline conductivity*  $K_N$  is low. The channel dematerializes (and opens) when the gate–channel voltage reverses enough to pinch the entire channel. This negative  $v_G$  is the *pinch-off voltage*  $V_p$ . So  $R_{CH}$  spikes sharply when  $v_{GS}$  and  $v_{GD}$  reach this  $V_p$ :

$$R_{CH} \Big|_{\substack{v_{GS} > V_p \\ v_{DS} \ll v_{GSP}}} \approx \left( \frac{L}{W} \right) \left[ \frac{1}{K_N (v_{GS} - V_p)} \right] \equiv \left( \frac{L}{W} \right) \left( \frac{1}{K_N v_{GSP}} \right) \equiv \left( \frac{L}{W} \right) R_{SH}. \quad (1)$$

This  $R_{CH}$  is more accurate when  $v_{GS}$  is uniform across the channel and above the pinch-off point. This happens when  $v_{GS}$  and  $v_{GD}$  or  $v_{GS} -$

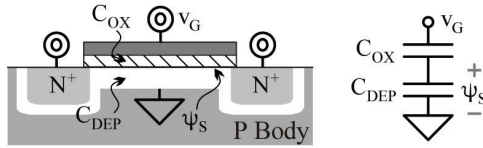
### A. Triode

$i_D$  rises with  $v_{GS}$  because a positive gate–source voltage reduces the gate–source barrier. This rise is exponential because  $v_{GS}$  avails exponentially more electrons than *junction temperature*  $T_J$  avails with  $V_t$ :

$$\begin{aligned} i_D \Big|^{0 < v_{GS} < v_{TN}} &= \left( \frac{W}{L} \right) I_{SN} \exp \left[ \left( \frac{C_{OX}''}{C_{OX}'' + C_{DEP}''} \right) \left( \frac{v_{GST}}{V_t} \right) \right] \left[ 1 - \exp \left( \frac{-v_{DS}}{V_t} \right) \right] \\ &= \left( \frac{W}{L} \right) C_{DEP}'' \mu_N V_t^2 \exp \left( \frac{v_{GS} - v_{TN}}{n_I V_t} \right) \left[ 1 - \exp \left( \frac{-v_{DS}}{V_t} \right) \right] \end{aligned} \quad (9)$$

$i_D$  also increases with  $v_{DS}$  because  $v_{DS}$  intensifies the field that pulls them to  $v_D$ . This  $i_D$  corresponds to *triode* because  $i_D$  is sensitive to  $v_{GS}$  and  $v_{DS}$ .

$i_D$  is high when  $W$  is wide,  $L$  is short, and the charge held in the *channel–body depletion capacitance* (per unit area)  $C_{DEP}''$  is high. These, *electron mobility*  $\mu_N$ , and  $V_t$  set the baseline conductivity of  $i_D$ .  $i_D$ 's *saturation current*  $I_{SN}$  combines the effects of  $C_{DEP}''$ ,  $\mu_N$ , and  $V_t$ .



**Fig. 16.** Voltage divider across gate oxide and surface–body.

The surface-to-body *surface potential*  $\psi_S$  in Fig. 16 is ultimately the voltage-divided fraction that  $v_G$  couples through the *oxide capacitance* (per unit area)  $C_{OX}''$  into  $C_{DEP}''$ , where

$$C_{OX}'' = \frac{\epsilon_{OX}}{t_{OX}} = \frac{3.9\epsilon_0}{t_{OX}}, \quad (10)$$

*permittivity in vacuum*  $\epsilon_0$  is  $8.845 \times 10^{-12}$  F/m, *relative permittivity of silicon dioxide*  $\epsilon_{OX}$  is  $3.9\epsilon_0$ , and *oxide thickness*  $t_{OX}$  is on the order of nanometers. The *non-ideality factor*  $n_I$  in  $i_D$  models the reduction in gate drive  $v_{GST}$  or  $v_{GS} - v_{TN}$  that  $C_{OX}''$  and  $C_{DEP}''$  cause. Surface imperfections

also re-assert another  $\psi_B$  in the opposite direction. Except,  $v_{SB}$  reduces this  $2\psi_B$  translation. And,  $v_{SB}$  alters  $|v_{TP}|$  by the amount that  $\gamma_P$  allows.

### 3.5. Symbols

The PMOS is a four-terminal device with interchangeable  $v_S$  and  $v_D$  terminals that conduct  $i_D$  in Fig. 33 when  $v_{SG}$  and  $v_{SD}$  are positive. The two vertical lines at the gate symbolize the  $C_{OX}$  that induces  $i_D$ .  $i_G$  is zero because dc current into  $C_{OX}$  is zero. So  $i_D$  is also the  $i_S$  that flows into  $v_S$ . The arrow attaches to the  $v_S$  that sets  $v_{SG}$  and points in the direction of  $i_S$ .

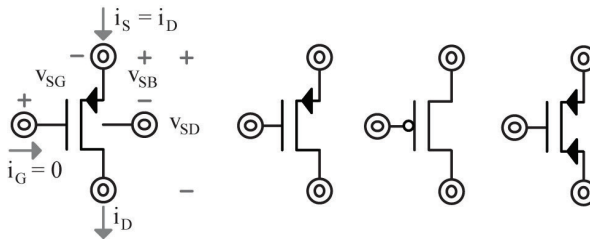


Fig. 33. P-channel MOSFET symbols.

The symbol sometimes excludes the body terminal to indicate other transistors share the same body. In these cases, independent access to the body is not possible. The arrow is also sometimes absent in digital circuits to show that source and drain terminals can reverse roles or on both terminals in switching power supplies to confirm that they will reverse roles. A "bubble" next to the gate distinguishes arrowless PFETs from NFETs. This indicates, like in a digital inverter, that PFETs "invert" the action of NFETs.

### 3.6. Unifying Convention

PFETs and NFETs function the same way. Accumulation, depletion, and inversion result when  $v_{GS}$  in NFETs and  $v_{SG}$  in PFETs are negative, positive and below  $v_{TN}$  and  $|v_{TP}|$ , and positive and above  $v_{TN}$  and  $|v_{TP}|$ .  $i_D$  saturates when  $v_{DS}$  in NFETs and  $v_{SD}$  in PFETs reach  $v_{DS(SAT)}$ ' and



disappear from  $C_G$  in Fig. 36. So  $C_G$ 's transition between  $2C_{OL}$  and  $C_{OX}$  is now monotonic with  $v_{SG}$ . The drawback to this *inversion-mode* varactor is that the  $v_{SG}$  range that changes  $C_G$  is usually narrow.  $v_B$  connects to the highest potential to reverse body PN junctions to  $v_S$  and  $v_D$ .

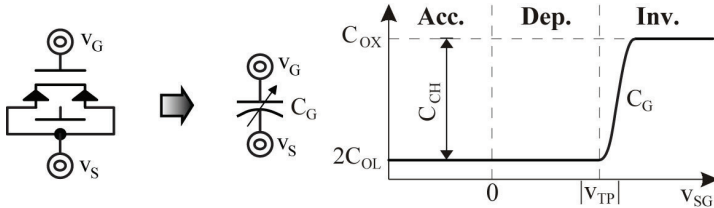


Fig. 36. Inversion-mode P-channel MOSFET varactor.

### C. Accumulation Mode

$C_{GB}$ 's transition in depletion in Fig. 34 is more gradual than  $C_{GS}$  and  $C_{GD}$ 's in inversion. A gradual transition is appealing because extending the voltage range that transitions capacitance is usually desirable in a varactor. So the purpose of the *accumulation-mode* structure in Fig. 37 is to eliminate the inversion mode from the bi-modal case.

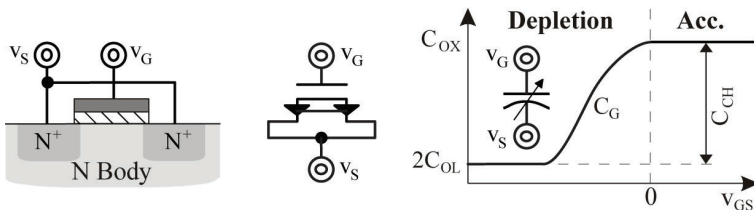


Fig. 37. Accumulation-mode N-channel MOSFET varactor.

The fundamental difference here is that the body is the same type of material as the source and drain. So the body connects the two  $N^+$  terminals when  $v_{GS}$  is zero – the line across the source/drain terminals of the NMOS in Fig. 37 represents this connection. A positive  $v_{GS}$  reinforces the connection because it pulls and accumulates electrons under the oxide. And a negative  $v_G$  repels electrons and depletes the

In PFETs,  $v_D$ 's field is so close to  $v_S$  that it pushes electrons away from the oxide region near  $v_S$  and presses nearby valence electrons into their home sites. Holes can therefore drift more easily. So PFETs also suffer a dynamic reduction in  $v_T$  when  $v_D$  falls.

### A. Thinner Oxide

The surface potential is ultimately the result of capacitor coupling from  $v_G$ ,  $v_B$  (via the body effect), and  $v_D$  (with DIBL). So in the absence of  $v_G$  and  $v_B$ ,  $\psi_S$  in Fig. 42 is the voltage-divided fraction that  $v_D$ 's depletion capacitance  $C_{JD}$  to the channel couples across  $v_G$ 's  $C_{OX}$ ,  $v_S$ 's  $C_{JS}$ , and  $v_B$ 's  $C_{JB}$ . DIBL is noticeable because short  $L_{CH}$ 's increase  $C_{JD}$ 's coupling.

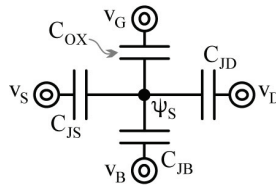


Fig. 42. Channel coupling components.

The effect of  $C_{OX}$ ,  $C_{JS}$ , and  $C_{JB}$  is to shunt  $C_{JD}$ 's coupling. So raising  $C_{OX}$  reduces DIBL. This is one of the driving reasons why engineers scale  $t_{OX}$  with  $L_{OX}$ . Another reason is higher current density  $i_D/W_{CH}$  and  $v_{GS}$ -to- $i_D$  gain because  $C_{OX}$  in  $K'$  climbs with reductions in  $t_{OX}$ . Reducing  $t_{OX}$  from 25 to 5 nm, for example, can suppress the 250-mV reduction in  $v_T$  that 100 mV across  $v_{DS}$  can produce when  $L_{OX}$  is 40 nm.

## 5.2. Gate–Channel Field

### A. Surface Scattering

Thinner  $t_{OX}$ 's intensify vertical gate–channel fields. So on their way to the drain, carriers accelerate and collide with the oxide on the surface of the semiconductor in Fig. 43 more often and with greater force. This scattering effect reduces *surface mobility* and produces noise in  $i_D$ . *Surface scattering* intensifies as  $L_{CH}$  and  $t_{OX}$  scale down.

activate them on purpose for their  $\beta_0$ . But this is not common practice, however, because they inject  $i_{\text{SUB}}$  into the shared substrate.

### C. Substrate MOSFETs

NFETs built directly over a P substrate share their body with the rest of the die. So independent access to their body terminals is not possible. Engineers sometimes use three-terminal symbols (in Fig. 22) to indicate this. In the case of substrate NFETs, the P body's connection to ground or to the most negative potential is implied. *Substrate MOSFETs* incorporate channel BJTs and substrate diodes.

### D. Welled MOSFETs

The body of PFETs built in N wells over a P substrate is the N well. So independent access to their bodies is possible. The four-terminal symbol (in Fig. 33) is therefore more appropriate and almost always used. On occasion, engineers use three-terminal symbols to indicate a pool of welled PFETs share one well and one body connection. *Welled MOSFETs* incorporate channel plus lateral and vertical substrate BJTs.

### E. Process Variants

Although less popular, integrating N- and P-channel MOSFETs in N substrates is also possible. In these cases, PFETs sit directly over an N substrate, NFETs lie in P wells, and the N substrate connects to the most positive potential. So PFET body terminals are not available.

Independent access to the body offers a degree of design flexibility that can help optimize and improve circuit performance. Substrate MOSFETs in "vanilla" *single-well* technologies do not offer this option. *Twin-well* or *dual-well* process technologies do because they can embed NFETs and PFETs in their own independent wells. The drawback is the additional expense of more fabrication steps.